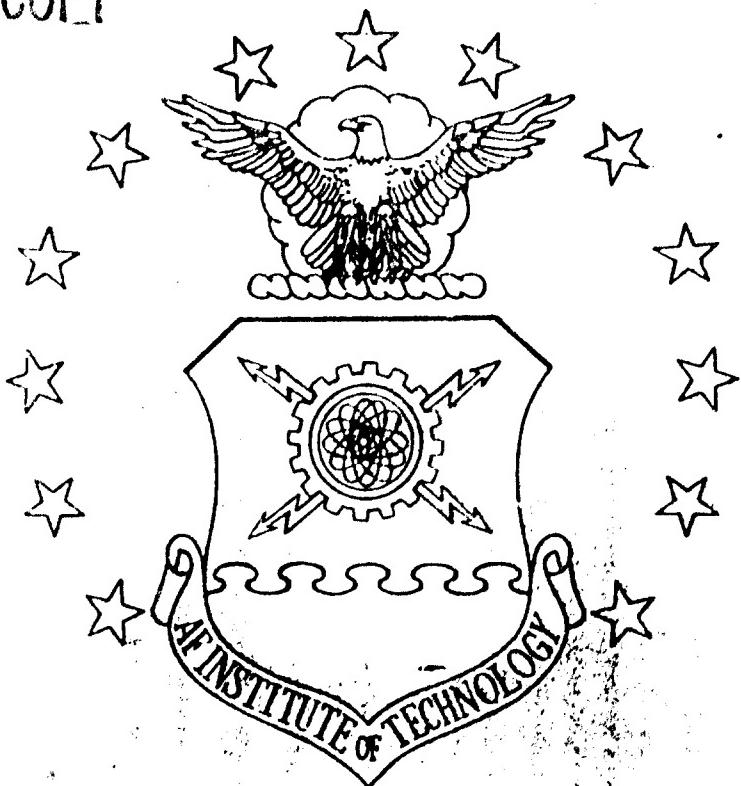


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DESIGN AND FABRICATION
OF AN
IMPLANTABLE CORTICAL SEMICONDUCTOR
INTEGRATED CIRCUIT ELECTRODE ARRAY

THESIS

Pierre K. LeFevre, Captain, USAF

AFIT/GE/ENG/90D-34

DEPARTMENT OF THE AIR FORCE
AIR UNIVERSITY
AIR FORCE INSTITUTE OF TECHNOLOGY

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Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
In Partial Fulfillment of the
Requirements for the Degree of
Master of Science in Electrical Engineering

Pierre K. LeFevre, B.S.E.E.

Captain, USAF

December 1990

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Preface

"You get these things in the same place you find frictionless pulleys, ideal point sources, and obedient children . . ." MK

What magnificent machines could be built if we could derive the blueprint of the mind. The ultimate goal of my thesis effort was to advance the AFIT brain chip to the point of a second implantation. My goal was almost reached. Unforeseen but not necessarily unexpected obstacles arose with each step of my thesis: software glitches; network down time; a loose proto-board connection; unsealed vacuum pumps; and ten thesis and doctoral students jockeying for use of the last operational machine.

Even though the work seemed helter skelter at times, it was fun at other times. I would like to thank Dr. Matthew Kabrisky, my faculty advisor, for the autonomy he allowed me in this effort, also for his help, and most especially for his contagious enthusiasm. "Thanks Matt!"

I would also like to thank Dr. Edward S. Kolesar, Jr. and Dr. Steven K. Rogers for their thoughtfulness and thoroughness with all of my thesis problems and questions.

My thanks to "Dr." Keith Jones and Russ Milliron for adding MAGIC to my life. Their instruction and help were invaluable.

The semiconductor laboratory could be a very dreary place if it weren't for Don "Smitty" Smith and Bill Trop. My thanks to them for keeping those "one-of-a-kind" machines operational.

My thanks to Pam Young for her light spirited humor that made those long days at AFIT bearable.

Also my thanks for the circle of support from the rest of the Semiconductor Devices Tract: Charlie Brothers; Bill Dolezal; Bob Fitch"e"; Dan Gaughan; Gene Graham; Rick Miller; Tony Moosey; and Steve Uyehata.

And finally I would like to thank my fiancè, Charlette, for her love and support through some long hours and short days.

Sincerely,

Pierre Ken LeFevre

"Good luck to you who follow on with this endeavor."

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Abstract

This research furthered the processing steps of the AFIT 16 by 16 implantable cortical semiconductor integrated circuit electrode array, or brain chip. The areas of interest include the brain chip electronics, metallization, ionic permeation, and implantation. The electronics and metallization are heavily covered.

A high speed, single clock divide-by-two circuit was modified with a reset transistor and cascaded to form a ripple counter. This device had stable operation at specific source voltage and clock voltage and frequency.

A 7-stage inverter with 10 unmodified divide-by-two circuits cascaded operated between 1.7 and 8 volts, and between 39 Khz and 1 Mhz, respectively.

The metallization process refers to coating Au/Ni or Pt onto exposed aluminum areas (pads) of a CMOS integrated circuit. Sputtering was used to coat the chip. And an Au/Ni etchant or Pt peel-off technique was used.

The Au/Ni etchant used was iodine, potassium iodide, and deionized water solution. Pt removal was accomplished by simply peeling the Pt up from the chip. Pt adheres to Al, but not to phosphosilicate glass (PSG).

The basic phenomena and operation of rubylith mask generation, photomasking, sputtering, and annealing are discussed in detail.

DESIGN AND FABRICATION
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IMPLANTABLE CORTICAL SEMICONDUCTOR
INTEGRATED CIRCUIT ELECTRODE ARRAY

I. INTRODUCTION

From a sea of strangers, we can find a familiar face. Through the din of a crowd, our name is immediately recognizable. With the first bite of a foreboding left-over patè, we can easily identify certain ingredients. These things are done almost effortlessly, but how? Part of the answer lies in an evolutionary new cortical sheath. This sheath, the neocortex of the mammalian brain, is assumed (by other neocortices) to be a transfer function equivalent.

Man's attempt to explain and determine this transfer function has led from simple hydraulic and mechanical analogies to more complicated theories of "nervous energy." Currently, the artificial neural network (ANN) is considered by some to function in a similar (albeit simplistic) manner as the neocortex (henceforth referred to as the cortex). However, regardless of the theory in vogue, a mathematical model may be developed by observing cortical activity.

Kabrisky and others (Kabrisky, 1966:40; Mittal, 1982:1140) proposed columnar computing units (vertically connected cortical neurons) within the cortex. These

computing units work together to perform complicated tasks such as pattern recognition. Using two Air Force Institute of Technology (AFIT) multielectrode semiconductor cortical implants (heretofore called the "brain chip", or simply the "chip" when the meaning is unambiguous), one to inject a signal into the columns and another to detect the outputs, a specific cortical processing model might be constructed.

Format to Assist the Reader

Because this thesis contains several areas of concern, the following format is used to assist the reader. All the identically titled sections, listed below, are related. To follow a particular area throughout this thesis, that particular section may be read independently of the other sections. The related sections are:

- Brain Chip Electronics.
- Metallization.
- Ionic Permeation.
- Implantation.
- Previous Result Problems.

Background

The brain chip project originated at AFIT in 1978 and has been implemented by a series of students and faculty research personnel. The chip is simply an input/output multiplexer. To simplify the discussion, this thesis will refer to the brain chip as an output device that multiplexes many signals

onto one output line from which they can be demultiplexed. The chip is designed to be a planar array of non-invasive electrodes connected to electronic gates.

The basic goal of this work is to place the chip onto the cortical surface. From this surface, the activity of the columnar computing units may be detected and/or influenced. Other research efforts used microelectrodes designed to pierce the cortical surface (Anderson, et al., 1989:693; Normann, et al., 1989:939; Najafi and Wise, 1986:1035; Mittal, 1982:1140). Some neuron degeneration will occur from the pressure and piercing. Dying neurons have been known to display signal anomalies, and crowded and damaged neurons might behave similarly. To minimize these effects, the brain chip will simply rest on the cortex.

Brain Chip Electronics. To keep up with technological and operational requirements, the multiplexer electronics have been updated and modified through many thesis efforts.

These electronics are required to reduce the tremendous wiring effort that would be required in a large multi-electrode array that hardwired each electrode into a private channel, such as the work reported by Demott (Szczublewski, 1989:2). In 1966, without the advantage of the newly developing semiconductor technology, Demott demonstrated a cortical array. The array consisted of a 20 by 20 set of wires directly connected through the skull with 400 leads. The AFIT brain chip circumvents the need for individual leads by multiplexing the implanted array's output.

In 1979, Joseph Tatman (Tatman, 1979:87) designed and a year later, Gary Fitzgerald (Fitzgerald, 1980:108) fabricated the first brain chip shown in Fig. 1. Set in a 4 by 4 array, each array element consisted of a gold electrode connected to a junction field effect transistor's (JFET) gate. All gates in a given row were connected so that any row of electrodes could be interrogated simultaneously. All gated outputs from a given column were wired to a single output connection.

Thus, by sequencing a "gate open" signal through each row, each row can be multiplexed through four column outputs. This basic design is also the heart of the second generation, 16 by 16 array.

In 1983, Robert Ballentine (Ballentine, 1983:I-6) redesigned the brain chip into a 16 by 16 array, using n-type

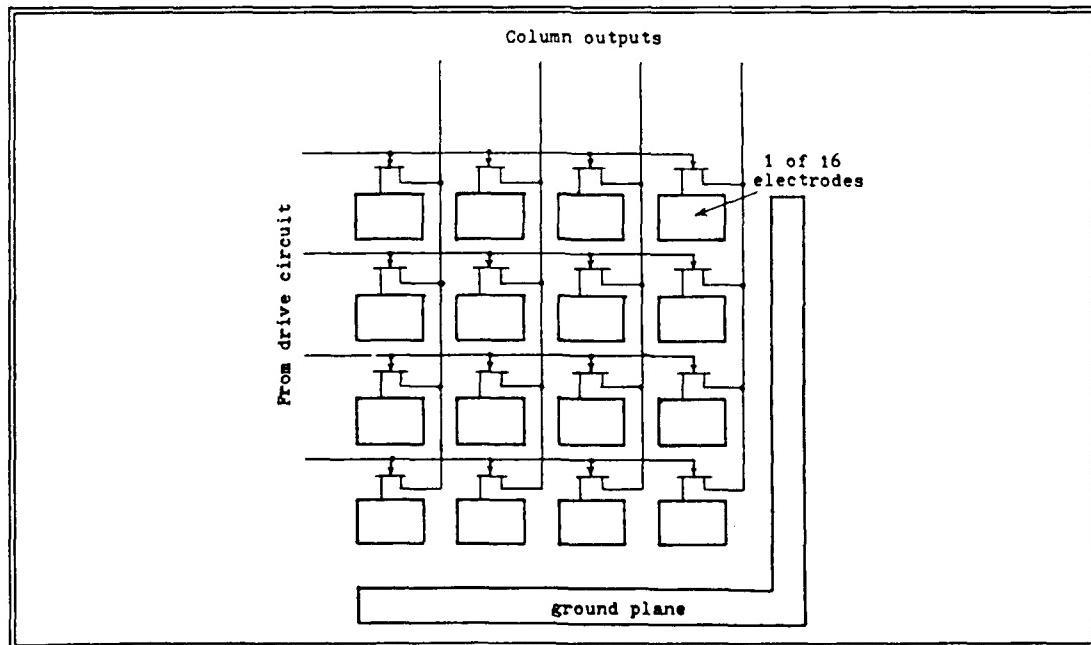


Fig. 1. Tatman's 4 by 4 JFET brain chip (Tatman, 1979:80)

metal oxide semiconductor (NMOS) technology (see Fig. 2). With the availability of very large scale integration (VLSI) technology and MOSIS (a VLSI contractor) fabrication, he included an onboard row sequencer and column output multiplexer. Thus, only one output lead was needed. Unfortunately, a design complication, attributed to appreciable polysilicon resistance, caused both the row sequencer and the column output multiplexer to malfunction.

In 1989, David Szczublewski (Szczublewski, 1989:11) redesigned Ballentine's chip into the current technology--complementary transistor metal oxide semiconductor (CMOS). To reduce design time, he eliminated the output multiplexer. After MOSIS fabrication, he discovered a malfunction in the row counter (part of the sequencer). Because of judiciously

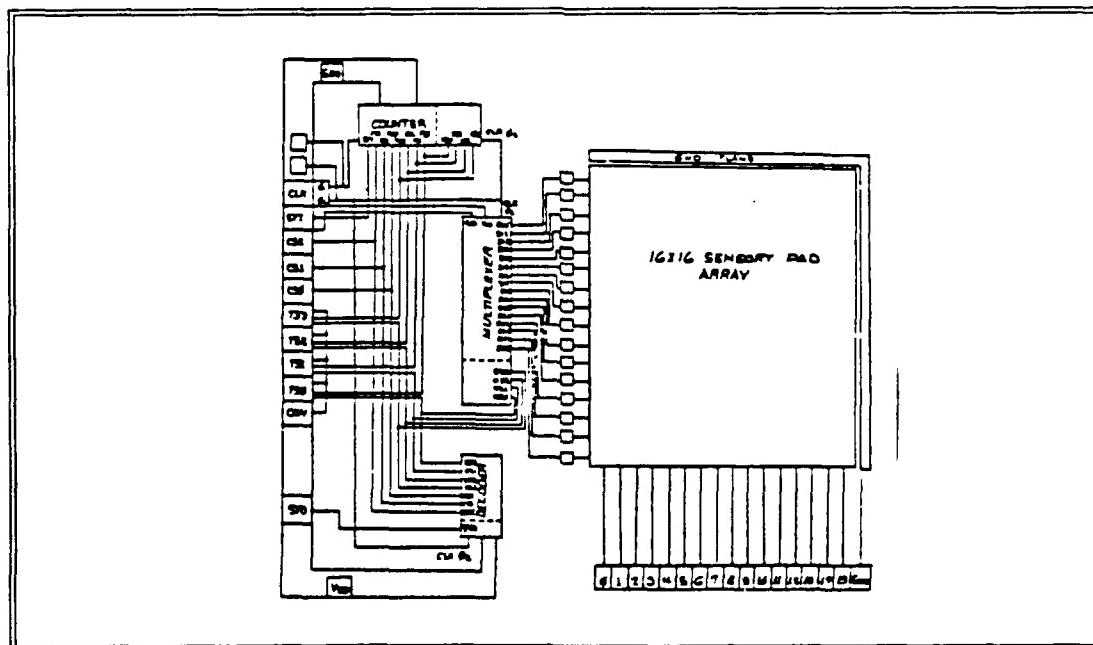


Fig. 2. General form of Ballentine's 16 by 16 NMOS chip (Szczublewski, 1989:22)

placed test pads, he tested and confirmed operation of the remaining portion of the sequencer and electrode gates.

Metallization. AFIT's JFET technology chips use gold conductors. Because gold resists corrosion in cerebrospinal fluid (CSF), Tatman's design had no corrosion problem. The current brain chip's primary disadvantage, is that MOS technology uses aluminum conductors. As a result saline can strip an aluminum electrode in a matter of days (Sedlak, 1986:141-3).

In 1984, Michael Sopko (Sopko, 1984:ix) designed and fabricated a 16 by 16 array made of gold electrodes and JFET gates. His procedure required a second chip to sequence each row. This procedure eliminated the corrosion problem, but it complicated the connection and packaging process.

Szczublewski (Szczublewski, 1989:89) tested various metal coatings on large scale (approximately $\frac{1}{2}$ inch square) aluminum electrodes, and decided gold was the best. Using various sputtering processes, he found that gold poorly adhered to aluminum. However, he corrected this problem with a nickel interlayer that strongly adhered to both gold and aluminum.

Because sputtering coats all exposed surfaces, the photomask, covered with metal, must be lifted off. The lift-off process leaves behind only the metal on the unmasked electrodes. Unfortunately, Szczublewski's sputtering process created excessive heat which caused his electrode photomask to permanently bond to the test wafer (Szczublewski, 1989:90).

Ionic Permeation. The brain is surrounded by CSF. This fluid contains sodium, potassium, and chloride ions. These ions can permeate transistor surfaces, thus impeding charge transport and eventually permanently disrupting the transistor's operation.

During saline (simulated CSF) tests, Fitzgerald (Fitzgerald, 1980:108-9) noted the need for a high quality passivation coating (a nonreactive, impenetrable surface). Using a passivating layer of silicon nitride, Tatman's chip failed after 30 seconds in saline. Fitzgerald conjectured that ions entered the chip through pinholes in the silicon nitride and concentrated in the high electric field areas associated with the transistor gates.

George German (German, 1981:G-59), as well as Steven Ernst (Ernst, 1986:5-1), tested various passivation materials. They concluded that polyimide (PI) would adequately protect the chip.

Russell Hensley and David Denton (Hensley and Denton, 1982:6) operationally tested Tatman's chip, using a PI coating. The test lasted 17 days over which the chip functioned properly, in effect no ionic permeation was noticeable.

Current AFIT coating equipment is not designed for handling the small MOSIS fabricated chips (less than one square centimeter). To alleviate this problem, Ricardo Turner (Turner, 1984:III-9-12) and Jeffery Sedlak (Sedlak, 1987:C-4) created procedures for coating small chips with PI. Testing

these chips in simulated CSF, again, confirmed the ionic transport resistance properties of PI.

Implantation. The brain chip must be easy to insert and remove. This reduces stress on the animal and allows visual inspection and modification of the chip as needed.

Hensley and Denton (Hensley and Denton, 1982:x,82) conducted the only implantation to date. Their procedure required surgery to both insert and remove the chip.

Turner (Turner, 1984:II-17) proposed a modified standard medical research implantation techniques. His method used a surgically implanted tube that penetrated the skull. This tube allowed nonsurgical insertion and removal of the chip.

To reduce stress even more, radio communication links were conjectured in Tatman's thesis and designed in Zeman's (Zeman, 1984:xi) thesis. A fully implantable brain chip would allow the animal to move about untethered by connection wires. With the scalp wound sutured shut, there would also be less chance of infection to the animal and damage to the chip.

Operational Results. Hensley and Denton (Hensley and Denton, 1982:x,36,81) tested Tatman's design on a laboratory beagle ("Ricky") in 1982. Testing lasted 17 days and confirmed that the chip could detect electroencephalographic (EEG) type signals. The visual cortex area was overlayed with the chip, and a strobe light was flashed into the dog's eyes. The output signal displayed typical visual cortex responses, thus confirming the feasibility of the basic chip design.

No injury or impairment of function to the dog was noticed during the 17 day period that the dog was on the brain reinforcement schedule. At the conclusion of the test, the chip was removed.

Ricky is alive and well at the time of this writing. He is now 17 years old.

Problem Statement

With each update to the chip, new challenges have arisen. The current set of challenges are stated below. Once these are satisfied, the current 16 by 16 brain chip should be operational.

Brain Chip Electronics. A 16 by 16 array requires 16 row inputs to provide signal gate way and 16 column outputs--32 external connections plus power lines. While there is a chance for misconnection if nothing else, the main difficulty with such a system is the large number of wires that must be threaded through the animals skin and skull. A row sequencer and column multiplexer would enable the elimination of 30 of these wires and would be very useful if the chip could be improved to the point where they functioned properly.

Further reduction of the external circuitry would also be of value. This would reduce impedance mismatch problems and test set-up time.

Metallization. Corrosion of the aluminum electrodes will contaminate the brain and destroy the chip; therefore, a biocompatible metal must be used to overcoat the electrodes.

Because the columnar signals of the cortex are less than 1 mV (Hensley and Denton, 1982:A-1), intermetallic resistances might become a significant factor. A theoretical model should be developed.

Ionic Permeation. The MOSIS chip must be coated to resist salt penetration and subsequent transistor corruption.

Implantation. To reduce trauma on the test animal, it would be useful if the brain chip was placed into a housing that allows nonsurgical insertion and removal.

Previous Result Problems (Szczyblewski, 1989: 93). Three row select lines (#0, #1, #2) were missing in the chip's design. Row #4 could not be selected. Finally, the electrodes were designed with the "PAD" command. MOSIS fabricates "PADs" with an interconnected double metal layer. The interconnections are small welds (micron sized holes) through the oxide separating the metal layers. The surface density of these holes might significantly reduce the contact area between the PAD and cortex.

Assumptions

Brain Chip Electronics. SPICE (circuit simulation software), ESIM (logic simulation software), MAGIC (VLSI computer aided design (CAD) software) and their results are valid.

Metallization. Gold and platinum are corrosion resistant in CSF. Contaminants introduced by sputtering are negligible.

Ionic Permeation. Polyimide provides excellent resistance to CSF contamination of the brain chip.

Implantation. The animal medical research laboratory has the expertise to perform the tube implantation surgery required in Turner's procedure.

Other. MOSIS semiconductor data are accurate. Previous theses results are valid.

Scope

The emphasis of this thesis effort was to combine previous thesis efforts to make the chip operational. Some of the procedures were modified to fit current material and machine availability. Due to time constraints, the Ionic Contamination, and Implantation sections were not completed.

Brain Chip Electronics. The output column multiplexer was a modification of the row sequencer. A clock was also added to the chip.

Metallization. An overcoating procedure for the Al pads was developed for Au/Ni, and platinum (Pt).

Low voltage transport properties through the interfaces (intermetallic resistance) have not been finalized at the time of this writing.

Ionic Permeation. The PI coating procedure was based on Takahashi's use of PI and compatible epoxy (Takahashi, 1987:70,72). This procedure was not adequately developed due to time constraints.

Implantation. Operational brain chip testing was not accomplished due to time constraints. The steps necessary for wire bonding were developed.

This thesis did not explore the area of radio communication links.

General Approach

Brain Chip Electronics. The CMOS row counter was designed using single clock delay elements and simulated using SPICE. This counter, along with the current row sequencer, was used as the basis of the column's output multiplexer. The finished design of the brain chip was simulated using ESIM.

Metallization. The whole metallization process including mask making, photomask application, sputtering, and metal removing was fine tuned.

Szczublewski's problem of excessively heating the lift-off photomask was eliminated by using a reverse etching technique. A technique for platinum lift-off was found.

Ionic Permeation. A PI coating procedure was unsuccessfully applied to two MOSIS chips. Further tests were not implemented due to time constraints.

Implantation. This was not accomplished due to time constraints.

Previous Result Problems. The three row select lines (#0, #1, #2) were redrawn. Row #4 problems were examined and corrected. The electrode "PADs" were replaced with a single

metal layer. (Unfortunately the MOSIS fabrication metal is only aluminum.)

II. CONSIDERATIONS

This chapter discusses some of the theoretical, design, and operational considerations involved with the brain chip effort. Only three major sections will be discussed: brain chip electronics; metallic corrosion; and ionic permeation.

Brain Chip Electronics

The preliminary reasoning, theory, design considerations, and simulations for the counter and clock are given in this section. All the chip electronic circuits were designed to operate at 5 V (V_{dd}) with the low voltage at ground.

A section on the chip's programmable input/output pads is included for reference.

Counter. The counter consists of three circuits: (1) reset inhibit; (2) clock inhibit; and (3) resetable divide-by-two circuits (Fig. 3).

The first circuit was a clock triggered reset inhibitor. The reset signal was only allowed to propagate during a clock transition. The negative transition was chosen, though a positive transition would have worked equally as well.

Once the reset signal passed, it was then allowed to inhibit the clock and "zero out" all the divide-by-two circuits. With this scheme, the reset signal would not shorten the "on" time of the last pad output before a reset occurred.

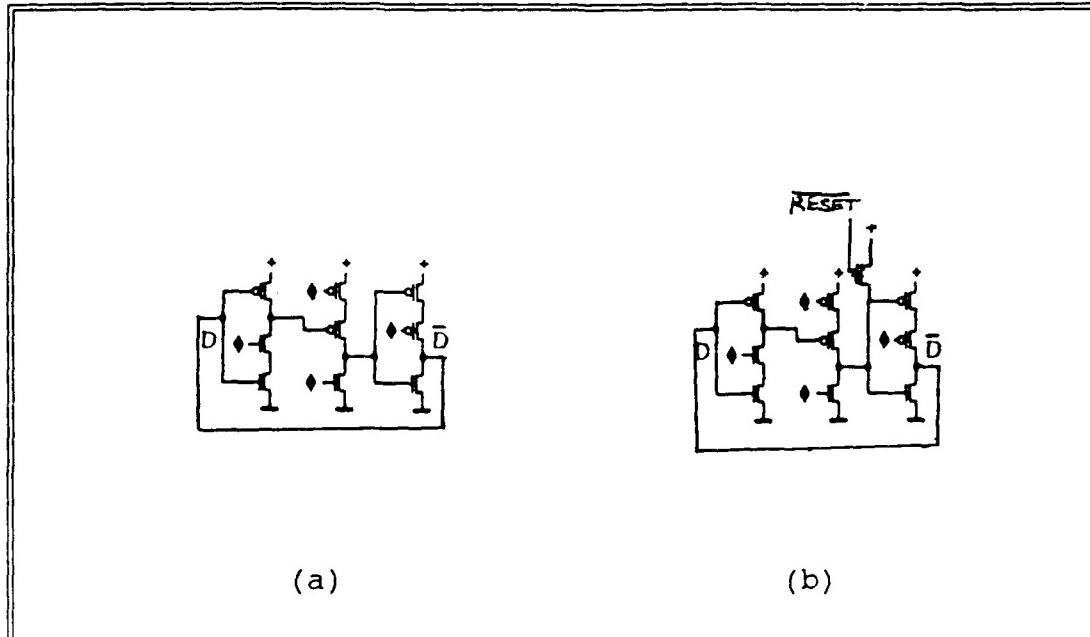


Fig. 3. Divide-by-two circuits: (a) nonresetable (Yuan and Svensson, 1989:65); (b) resetable

To allow the use of a single nonoverlapping clock pulse, the divide-by-two circuit suggested by Yuan and Svensson (Yuan and Svensson, 1989:68) was chosen (see Fig. 3 above). Their divide-by-two circuit allows operation in the 100 Mhz range. Thus, they could sample a very large array (333 by 333) (explained in the Clock section below). The circuit was also chosen to trigger on a negative clock pulse. Again a positive triggering circuit could have been chosen.

SPICE simulations were not reliable when three or more divide-by-two circuits were cascaded together. With three circuits, an erratic signal appeared on the third circuit's output after it went high (to V_{dd}). With four or more circuits, calculation errors halted the SPICE program.

To allow each circuit to be resetable, a reset transistor was added (see Fig. 3 above) and simulated. Again, when cascaded, SPICE had the same problems as it had with the original circuit.

Row selection was determined by the binary number (ra3)(ra2)(ra1)(ra0). Ra1, ra2, and ra3 are the outputs from the first, second and third divide-by-two circuits, respectively. Ra0 is directly connected to the CLOCK input line.

Clock. The clock design used a ring oscillator and ten Yuan and Svensson (non-resetable) divide-by-two circuits (figure). The ring oscillator was chosen for two reasons: simple design (seven inverters); and small area. The divide circuits allow the oscillator to run at a higher frequency. This reduces clock errors, caused by oscillator variations, by averaging up to 2^{10} (= 1024) (due to 10 divide circuits) oscillations before producing one clock pulse.

The collective output firing rate of the neurons in the columnar computing units is on the order of 50 Hz. But the clock frequency should allow a minimum sampling speed of 1 KHz for each brain chip array pad. This reduces alternating current (AC) impedance so the small amplitude columnar signal can more easily pass.

Because the ring oscillator's frequency would not be exactly known until it was electrically tested, the last four divide-by-two circuits were connected to output buffer pads and the counter's clock input was connected to an input pad.

This would allow a usable oscillator frequency to be hardwired after fabrication. The oscillator simulated at approximately 70 MHz on SPICE. With ten divide circuits, the frequencies of the last four circuits were approximately: 546 kHz; 273 kHz; 137 kHz; 68 kHz.

Programmable Input/output (I/O) Pads. This section is included because these are not standard AFIT input/output pads, and no information was available. This I/O PAD is located in the file: "ioP.MAG". These pads can ground excessively high voltage input signals to the chip and buffer the chip's output digital signals. The input signal path is hardwired from the pad to an input line (labelled IN on MAGIC files) to the chip electronics. The output has a separate output line (labelled OUT) from the chip electronics to the pad, but this path is buffered. The buffer is electrically programmable through the enable line (labelled ENB). The ENB line programs as follows:

ENB = highest chip voltage (V_{dd}) = buffer enabled

ENB = lowest chip voltage (gnd) = buffer disabled

Metallization

This section will discuss the metallization process, including photomasking, sputtering, metal removing, and annealing.

Photomasks. Organic polymers can be used as photomasks. These polymers are suspended in organic solvents (Maissel & Glang, 1970:183). Because the polymers have poor wettability

on a silicon (Si) or silicon dioxide (SiO_2) substrate (wafer or chip), a wetting agent (adhesion promoter) must first be applied to the substrate. Spinning the substrates is a typical way to apply these liquids (adhesion promoter and photomask). This spinning process a somewhat uniform layer with estimateable (knowing spin speed and liquid viscosity) thickness and partially dries the liquid for subsequent applications.

Photosensitive polymers (resists) are usually ultraviolet (UV)-sensitive plastics. These resists are typically used as photomasks and fall into two categories: negative and positive.

Negative resists form strong bonds when exposed to UV light. This allows the exposed areas to withstand subsequent rinsing (development). The shaded areas wash away.

Positive resists initially form strong bonds. UV light causes these bonds to break. Thus the opposite condition occurs during development. Exposed areas wash away and shaded areas remain.

By forming a pattern in black or its reverse image in clear (nonpattern areas in black), either resist may be used. This pattern would be placed over the substrate and then exposed to UV light. The UV-light will transfer the pattern to the resist. And upon development, the transferred pattern would be visible. This pattern is the photomask.

Sputtering. Sputtering occurs when ions bombard a target material knocking off the target's atoms. These atoms fill

and coat the inside surfaces of a sputtering chamber. The type of sputtering using radio frequency (RF) energy was used in this thesis.

RF Sputtering. This section is summarized from Maissel & Francombe, 1984:55-57. The most efficient RF frequencies are between 1 Mhz and 2 Mhz. But these frequencies interfere with communication transmissions. Therefore, the Federal Communications Commission (FCC) has allotted specific frequencies for RF sputtering, the lowest being 13.56 MHz .

To get the maximum power into the RF field, an impedance matching network must be used, otherwise excessive power may be reflected back into the RF generator. Typical RF generators have an internal impedance of 50 ohms. The discharge load is typically much less and includes the target resistance and space charge capacitance (an area of separated charge between target and plasma). A capacitor is also placed in series with the load to allow the target to self-bias (a process described below).

Ions used for bombardment are supplied by chemically inert gases such as argon (Ar). The inert gas ionizes due to the RF field energy exciting its electrons. The excited electrons sometimes fall back to a lower energy level, creating the plasma glow. The excited electrons that escape then follow the periodic RF field lines. The heavier gas ions react much slower to the changing RF fields lines.

The freed electrons near the target quickly gather on the target, charging it negatively. This charging is called self-biasing; it halts further electron charging and attracts positive ions. The attracted ions bombard the target dislodging target atoms.

Some dislodged target atoms become ionized and are attracted back to the target, possibly dislodging more target atoms. Other target atoms dislodge with enough energy to escape the target's surface. These escaping atoms travel a relatively undisturbed path. Dispersive effects are caused by collisions and field effects (on target ions).

Because of the alternating fields, sputtering can occur on the substrate. However, because of self-biasing, target sputtering occurs considerably more often than substrate sputtering. Contamination due to substrate sputtered material becomes inconsequential after the substrate becomes coated by target material.

Deposit Formation. Sputtered material deposits on the substrate in droplets (Fig. 4a). These droplets increase in size forming islands of different grain orientations (Fig. 4b) (Maissel and Glang, 1970:13-31). The initial grain size roughly depends on the melting point of the deposited metal; higher temperatures correlate to smaller grains (Einspruch, 1986:226). The islands eventually join, but grain boundaries still exist (Figs. 4c, 4d)

Operational Considerations. Contamination, defect densities and heat generation are controllable factors in

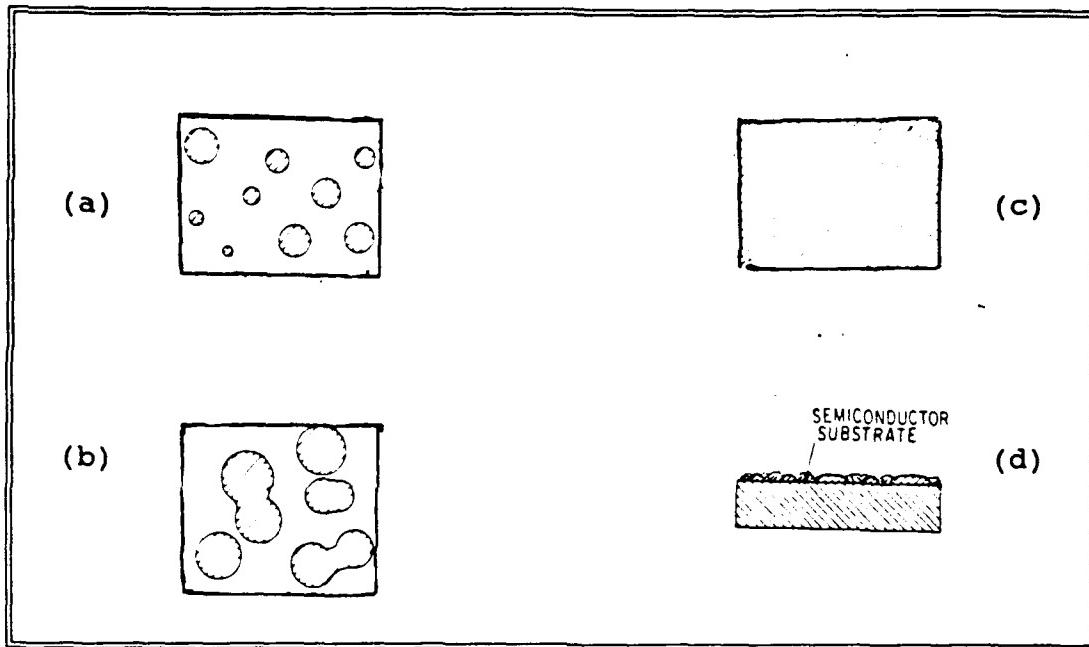


Fig. 4. Deposit Formation: (a) target droplets; (b) droplet agglomeration; (c) formation of continuous sheet; (d) side view of continuous sheet (Einspruch, 1986:230)

sputtering. Low starting pressures (less than $2 \cdot 10^{-5}$ Torrs for Al sputtering) are required to reduce atmospheric gaseous contaminates to a negligible amount. At this pressure an inert gas is added to the chamber to allow contamination free sputtering.

The remaining gases and added inert gas can become trapped within the sputtered material. This could impede lattice formation; however, high background pressures of the inert gas combined with slow deposition rates tend to reduce structural defects (Maissel and Glang, 1970:13-28), possibly due to more uniform scattering (coating) of the sputtered material. Slow deposition rates also allow the heat

(generated by target atom impact) to dissipate, thus keeping substrate temperatures lower.

Contaminates on the target can be removed by presputtering (target covered by the shutter) for several minutes. Substrate contaminates must be removed beforehand.

Metal Removal. Two standard methods were tried: lift-off and etching.

To lift-off the undesired metal, a photomask is first applied to the substrate. The photomask is a negative image, covering the areas where metallization is undesired. The applied photomask must be well developed with sharp corners and walls higher than the thickness of the metal layer applied. These two factors will determine how successful the lift-off will be. After the metal is applied, the photomask is removed by an organic solvent. The walls, if steep enough, will be covered with a very thin, if any, layer of metal. Since this is the weakest point, the metal will break at the walls when the photomask is removed. Thus the metal covering the photomask will simply lift off.

Etching is done in a reverse manner. First the metal is applied, then the photomask (this time the positive image is used, covering the areas where the metal is desired), and finally the undesired (exposed) metal is removed with a metal specific etchant.

Annealing. Heat treating or annealing can have many effects on the metal/metal interface. Desired annealing temperatures and application time will vary with the interface

metals and defect densities. In all cases the temperature should be kept below the lowest melting point of all materials on the chip.

Interface Metals. Specific interface alloy or compound formations are favored at specific temperatures and annealing time. To assist in temperature selection, a set of graphs showing the equilibrium diagram of specific alloys (Al-Au, Al-Ni, Al-Pt, Au-Ni, and Au-Pt) is included in the appendix: Alloys. From this appendix, the eutectic temperature can be found.

The eutectic temperature is the lowest alloy melting point temperature (Sze, 1985:372). It indicates the temperature required to combine one metal's atoms into the other metal's lattice structure. Below this temperature the two metals will only diffuse through, without becoming part of, each others lattice structure.

The Ni/Al interface composition is described by Colgan and Mayer (Nemanich, 1986, 121-126). Al diffusion dominates and initially mixes into the Ni layer at 250 °C. Should the Ni layer, in the Al/Ni/Au electrode pad, be too thin, Al could diffuse into Au causing a known detrimental phenomena, the "purple plague".

Compound formation of AuAl_2 is implicated in "purple plague". The "plague" appears as a very dark purple or black formation growing from Au toward Al. The activation temperature to form Au/Al compounds is 164 °C. At this temperature the primary compounds formed are Au_2Al and AuAl_2 .

Some studies implicate Si atoms act as a catalyst for AuAl₂ formation (Cunningham, 1965:737~741). Temperatures as high as 250 °C might occur on the substrate surface when sputtering at a high deposition rate (Szczublewski, 1989:63).

The "plague" phenomena manifests as a loss of mechanical adhesion between Au and Al. The cause is a large diffusion of Au into the Al to form AuAl₂. And appears as separations, voids, and cracks around the Au/Al interface.

Some of AuAl₂'s characteristics are: a small resistivity at room temperature of 7 $\mu\Omega\text{-cm}$; a cubic crystal, set in a fluorite structure; a lattice constant of 5.99 Å; and a bright purple color (Jan & Pearson, 1963:280-283).

Defects. Two ways defects can form are by high deposition rate and contamination.

High deposition rates do not allow the metal atoms time to form a uniform lattice structure. Lattice nonuniformities (not including contamination) occur through vacancies (missing lattice atoms), interstitials (extra atom within lattice structure), and dislocations (skewed lattice structure). Vacancies and interstitials will migrate toward each other at room temperature, but the extra (interstitial) atom will not move into the lattice vacancies until the proper annealing (activation) temperature is reached (Maissel & Glang, 1970:13-26).

Two representations of a skewed lattice structure are fissures and grain boundaries. These could allow gas and liquid influx, possibly resulting in corrosion and oxidation.

Annealing will cause the grains to coalesce forming fewer but larger grain boundaries (Einspruch, 1986:226). Filling of the fissures should occur at high enough temperatures, but surface tension will cause beading if the top metal film is less than a few hundred angstroms thick (Maissel & Glang, 1970:13-31).

Atomic contaminants may become carrier trap sites. But annealing will cause them to diffuse and reduce their effect. Large contaminants will not move and reduce contact area, reducing adhesion and current flow. Also a build-up of oxides on substrate, if nonconductive, will increase resistivity.

Sometimes the defects can reduce resistivity by adding energy states inside the interface barrier. This can assist both thermal and tunneling electron currents.

:
Ionic Permeation

This section contains array pad masking considerations and polyimide considerations.

Array Pads. To reduce ionic permeation (leakage) into the silicon substrate between the Al array pads and the phosphosilicate glass (PSG), the PSG windows, metal overcoats, and PI windows varied in surface area. The PSG windows were undersized by 10 μm in length and width to 160 μm by 160 μm . The metallization masks were oversized to 180 μm by 180 μm . And the pads on the PI mask were again undersized to 160 μm by 160 μm . These variations would help to ensure that all seams were completely covered.

Polyimide. Polyimides are highly useful as the final coating for the brain chip. They provide resistance to moisture (by absorbing several times their weight in liquids), solvents and acids. They will planarize over an uneven surface, filling small gaps and smoothing steps. And they have a low dielectric constant (≈ 3.5); and a typical leakage current of 10^{-12} A in a field strength of 4.5 kV/cm. These properties depend on the polyimide's precise molecular formulation and curing process (Mittal, 1982:648).

During curing two action take place--loss of solvent and chemical reactions between solvents. This results in loss of volume and creates stresses. But if cured at the "glass transition temperature" (400°C), polyimides become plastic and internal stresses are relieved (Mittal, 1982:701).

III. METHODOLOGY

This chapter contains information about setting up specific processing steps. Preliminary results, design efforts, and standardized methods are included.

Brain Chip Electronics

This involved the following: designing a counter, output multiplexer and clock; simulating the design; and electrically testing the fabricated chip.

Design. The electronics were designed and fine tuned using SPICE simulations.

The row sequencer was modified with a newly designed counter. The counter was a modification to the divide-by-two circuit of Yuan and Svensson (Yuan and Svensson, 1989:68). Synchronous clock and reset circuits were attached to the front end of the counter; and a reset transistor was added to each divide-by-two circuit.

The output column multiplexer was used to operate column output transmission (T) gates. It consisted of a resetable divide-by-two circuit connected to the CLOCK input of another row sequencer circuit .

The clock design used a ring oscillator made of seven inverters and ten divide-by-two circuits to even the pulses and reduce the frequency.

Simulation. The counter was simulated using SPICE and ESIM. The whole chip (excluding the clock) was then simulated using ESIM. All connections, inputs and outputs were labeled on the MAGIC display to facilitate simulating and troubleshooting.

The oscillator with two divide-by-two circuits was simulated on SPICE. Because ESIM does not simulate feedback circuits, only the divide-by-two circuits were digitally simulated.

Fabrication. The completed VLSI design (MAGIC file designated, MONKEY5.MAG) was converted to a file compatible with the current MOSIS production format. This was done through the MAGIC "CIF" (Caltech Intermediate Format) command. The converted file (MONKEY5.CIF) was attached to an authorization letter, and electronically mailed to MOSIS. Attached to the letter was a request that half of the brain chips be packaged. The packaged chips facilitated electronic testing. MOSIS bonded them into a 132 pin package.

Testing. A test package was built. It consisted of a zero-input-force (ZIPF) holder wire wrapped to proto-board compatible pins. (Fig. 5) Each connection on the test package was individually tested for continuity.

For the initial power-up each of the chip's inputs and outputs were sinked to ground through individual 5.1 K ohm resistors. The voltage was then slowly brought up from ground to 5 V (V_{dd}). And the current into the chip was calculated by

ground		1 14	column 1 output
--		2 13	column 2 output
source voltage		3 12	column 3 output
--		4 11	column 4 output
--		5 10	column 5 output
ra0 row		6 9	column 6 output
ra1 address		7 8	column 7 output
lines			
ra2		1 14	column 8 output
ra3		2 13	column 9 output
--		3 12	column 10 output
RESET input		4 11	column 11 output
--		5 10	column 12 output
TOP ROW SYNC		6 9	column 13 output
1st COL SYNC output		7 8	column 14 output
ROW16 COL16 SYNC output		1 14	column 15 output
--		2 13	column 16 output
/128 clock		3 12	--
/256 output		4 11	MUXED_OUTPUT
/512 (frequency		5 10	--
/1024 dividers)		6 9	--
CLOCK input		7 8	ground strip output

Fig. 5. Top view of pin-out for test package for MOSIS chip,
the labels are descriptive and correspond to MAGIC labels

the voltage drop across a 5.1 K ohm resistor in series with
the voltage input.

"Destructive" testing was done with the acoustic cutter.
Various metal lines on the chip were cut to determine their
effect on the counter's operation.

Metallization

The interface current flow test set-up, along with
processes involving cleaning, coating and masking the wafers
and chips are discussed in this section. Further descriptions

of these processes and equipment used are found in various appendices.

Contamination. Contamination is a very critical factor when metallizing. To remove contaminants the standard cleaning schedules from previous thesis were used and modified for this thesis (see appendix: Standard Cleaning Schedules). Positive air flow through filtered hoods, bottled nitrogen and argon, filtered deionized water (DIW) and covered containers were all used in an effort to reduce contaminates.

Masks. The mask generation process required rubylith masks to be cut, reduced to chip size on glass plates, and multiple copies made.

Rubylith Process. Rubylith was used to generate a mask. This process involved making a mask many times larger than the desired size and photo reducing it. Because of tolerance errors, the array pad openings were cut either slightly larger or smaller, as needed. Slightly larger openings allowed complete coverage of the array pads. This was necessary when overlaying the pads with a biocompatible metal. Slightly smaller openings ensured the array pad edges would not be covered. This ensured that there would be no gaps between the PI coating and the array pad edges.

The rubylith mask was designed and fabricated as follows: for ease of handling (around 2 feet on each side), MAGIC coordinates were scaled up by 70 times, then converted to inches for the rubylith cutting table (see appendix: Mask Coordinates). The rubylith was smoothed down on the table

with the rubylith side face-up. Then the cutting blade was aligned and tightened. The cuts were made in a checkerboard fashion to reduce cutting time. And the pad areas were peeled off.

Plates. Plates are simply a photographic emulsion placed on a glass backing. The emulsion side is toward the smooth edge of the glass. The smooth edge can be determined by running one's fingers along the edge (either top, sides, or bottom). A roughness will be felt either toward the front or back of the plate. The other side will be smooth. This is the emulsion side.

Variable Reducer. The variable reducer will reduce an image up to 70 times. The calibrated reduction size of 70 times was used. The settings were 87.0000 for the rear box (closest to eyepiece) and 67.7590 for the front box (closest to rubylith). The 35 mm wray lens was required for this reduction size.

The eyepiece was used for fine adjustment of the lens. To do this, the eyepiece was first focused on the emulsion side of a plate (emulsion set toward the rubylith). The emulsion contained scratches on it to facilitate focusing. Then the rubylith image was brought into focus by moving the front box (toward rubylith) of the reducer. Once done, the eyepiece was used to roughly confirm the reduction size by measuring the image (1 turn was approximately 25 mils (1 mil = .001 inches)).

The emulsion side of the plate is placed toward the rubylith to allow the best image definition. By placing the emulsion on the surface toward the rubylith, the rubylith image will not diffract through the plate.

Reverse Plate Copier. Because chip and wafer processing could damage or contaminate masks, the reverse plate copier was used to make copies of the best masks. The copier creates a reversed, mirror image; therefore, a copy of the reverse, mirrored copy was required.

Several combinations of copier setting were tried. The settings used were:

exposure time:	10.0 s
photoresist intensity:	6
emulsion intensity:	4
plate separation time:	2
vacuum pumpdown time:	1
N ₂ purge time:	2
lamp servo:	normal

Exposure time was the most influential setting. Short exposure times resulted in non-opaque masks. Small separations in plate contact resulted in Newton ring formations. Longer exposure times allowed light leakage into covered areas.

Plate Developing. Fresh chemical baths allowed the most definition and contrast. The typically used development sequence was 3 minutes in developer, 1 minute in stop, 1 minute in fixer, several minutes in a DIW rinse, and then

gentle blow drying with N₂. Contaminates were kept to a minimum by holding the plate in a dust filtered hood with the emulsion side down.

Photomasks. The photomask processes included applying, exposing, developing, and removing the photomask.

Application, Exposure, and Development. Before any coating procedures were done the appropriate procedure in the appendix: Standard Cleaning Schedules was performed.

Previous theses used Shipley 1350J positive photomask, Shipley 351 developer and deionized water (DIW) as a stop. These were tried with a similar procedure given in previous theses. The mask aligner was set for a 30 second exposure, and development proceeded in 30 second or longer intervals. The chips were spin developed at 1 or 4 krpm. This method was abandoned because not all pads could be completely cleared of photomask.

Shipley 1450J positive photomask was used. This was a dark liquid (Shipley 1350J was clear) that absorbed scattered light to allow sharper photomask definition. It also required an adhesion promoter. Hexamethyldisilazane (HMDS) was used. Various spin speeds were tested.

After applying the photomask, the chips were softbaked. Softbaking dries the surface and allows mask contact without sticking.

Various exposure times and development spin speeds were tried. The development process consisted of 1 minute steps done until the exposed areas of the positive mask were

removed. The steps included: about 20 seconds of spraying with developer; about 10 seconds of spraying with stop (DIW); 30 seconds of spin drying at 5 krpm; and then a visual inspection under the microscope. The developer used was Shipley 312A in a 4:3 solution with DIW.

Removal. Microposit 303A (developer) was used in a straight 1:0 solution to completely strip Shipley 1450J photoresist.

Other possibilities for photomask removal were commercial removers (solvents), plasma ashing, and ultrasonic agitation. To remove Shipley 1350J positive photomask, a Shipley technical representative suggests remover #1165. Plasma ashing chemically reacts an appropriate gas plasma with the photomask to form a gas. The gas is then exhausted. Commercial removers and plasma ashing were not used.

Ultrasonic agitation was tried for removal of the photomask. Several chips and wafers were set into an acetone bath and placed into the ultrasonic agitator.

Spinner Modification. This device senses the vacuum pressure at the chuck opening. To spin a chip, the smallest chuck was pushed onto the spinner shaft. Then a piece of vinyl tape, with a small hole cut in the center, was centered over the vacuum opening. The vinyl tape should seal around the chip and allow the spinner to operate.

Mask Aligner Height Adjustment. There are several mask aligner adjustments available: height of the wafer holder; vertical, horizontal, and skew holder movements; mask

holder bracket; and exposure time. The height was adjusted by: (1) placing the chip or wafer onto the wafer holder; (2) loosening the mask holder bracket; (3) moving the wafer holder lever down and pushing the contact holder away; (4) rotating the height adjustment until the wafer or chip just touched the mask, then lowering just a bit; (5) and finally tightening the mask holder bracket down.

Bringing the wafer holder to its lowest point, then turning twice past zero and stopping around 1.00 was found to be a typically used height setting.

Sputtering. Metallization techniques were developed using wafers, and previous and current brain chips. This section includes target set-up, sputtering operation, thickness measurements, and sputtering temperatures.

Vacuum Preliminary Set-Up. The "O"-rings were critical to creating and maintaining a good vacuum. Malformed and pocked rings were replaced. The ring pockets were cleaned with high-vacuum greased Q-tips. The rings were wiped clean, then lubricated with high vacuum grease. Before tightening down the targets, the chamber was tested for leaks by evacuating the chamber to a pressure of a few microns of mercury.

Operation. The cyropump required an extensive cooling system and two or more hours to cool down to an operating temperature. Before sputtering the vacuum was allowed to reach below .02 m Torr. This eliminated most of the airborne contaminates.

The RF sputtering system was powered at the circuit breakers. It also had an interlock located on the rear door. The interlock was clamped down and the rear door was opened for cooling purposes.

The Ar gas solenoid would not always open at Ar pressures more than 20 psi. (A "clink" was heard when the solenoid opened.) And the target closest to the Ar port was found to react quickly to changes in Ar pressure. The discharge pressure gauge, being further away from the Ar port, had a delayed reaction to the pressure changes.

The targets was covered for several minutes when sputtering first begins. This removed most target surface contaminants (substrate surface contaminants were removed previously in the Standard Cleaning Schedules: Aluminum Cleaning this reduces the highly resistive aluminum oxide). Initial sputtering onto the substrate was done at a slow rate (low RF power). This slow build-up at the metal interface reduced structural defects and allowed better metal adhesion.

Thickness of Deposit. To monitor the deposition rate and thickness on a substrate during sputtering, the thickness monitor was used. Three constants were needed: material density; acoustic impedance; and tooling factor. The material density and acoustic impedance are listed in the section appendix: Metallic Constants. The tooling factor was simply a multiplying factor to compensate for the different placements between substrate (item to be coated) and monitor.

A first estimate of the tooling factor was given in the

thickness monitor manual as the square of the following: distance from target to monitor divided by the distance from target to substrate. The tooling factor was refined by measuring the actual thickness of the sputtered material. The substrate was placed half way between both target on.

By placing the chips on a flat material (specimen slide or wafer), the sputtered material built-up around the chip. The sputtered ledge was measured using the DEKTAK II measuring machine. This resulted in a tooling factor of 600% for the Au and Pt targets.

Temperature. Because of Szczublewski's problems with excessive heat, a thermocouple was initially used. It was connected to the substrate platform and observed during a sputtering session. Unfortunately the plasma disrupted the thermocouple's output. However, after the plasma was halted the temperature reading was 63 °C. This was after 1 hour of Ni and 20 minutes of Au sputtering. The chamber was hot to the touch.

Metal Removal. An Au etch of iodine (I_2) and potassium iodine (KI) was used in the following proportions:

1 g of I_2 : 4 g of KI : 40 ml of DIW

To remove Pt from the PSG, photomask was applied to the Pt after using the Surface Cleaning schedule. The photomask was softbaked, then tape was smoothed over the chip with a cotton swab and pulled back at a 180° angle.

A brand name tape (Scotch) was used because generic tape had a tendency to break apart possibly due to nonuniform tape thickness.

Metal Adhesion. Scotch tape removal tests were performed on the Ni/Au and Pt plated chips. The test involved smoothing the tape onto the chip with a cotton swab then pulling the tape off at a 180° angle (Szczublewski, 1989:64).

Annealing. Sputtered Pt was annealed to allow the Pt/Al interface to form a more uniform structure. The annealing was done at 250 °C for 48 hours in the laboratory oven. Higher temperatures were not tried because Szczublewski found that annealing at 350 °C for 2 hours caused the Pt/Al interface to separate upon tape removal (Szczublewski, 1989:66).

Pad Sensitivity. This was tested after the metallization. The test applied a square pulse through the ground strip and ground strip output pad. The set-up is shown in Fig. 6.

Ionic Permeation

Time did not permit this section to be fully explored.

Polyimide. The mask for the PI was designed to overlay the pads, ideally, by 10 microns. If the PI only abuts the edge of the pads, fissures, between PI and pads, could then form allowing CSF influx.

Time did not allow development of an application procedure for Takahashi's (Takahashi, 1987:157) polyimide.

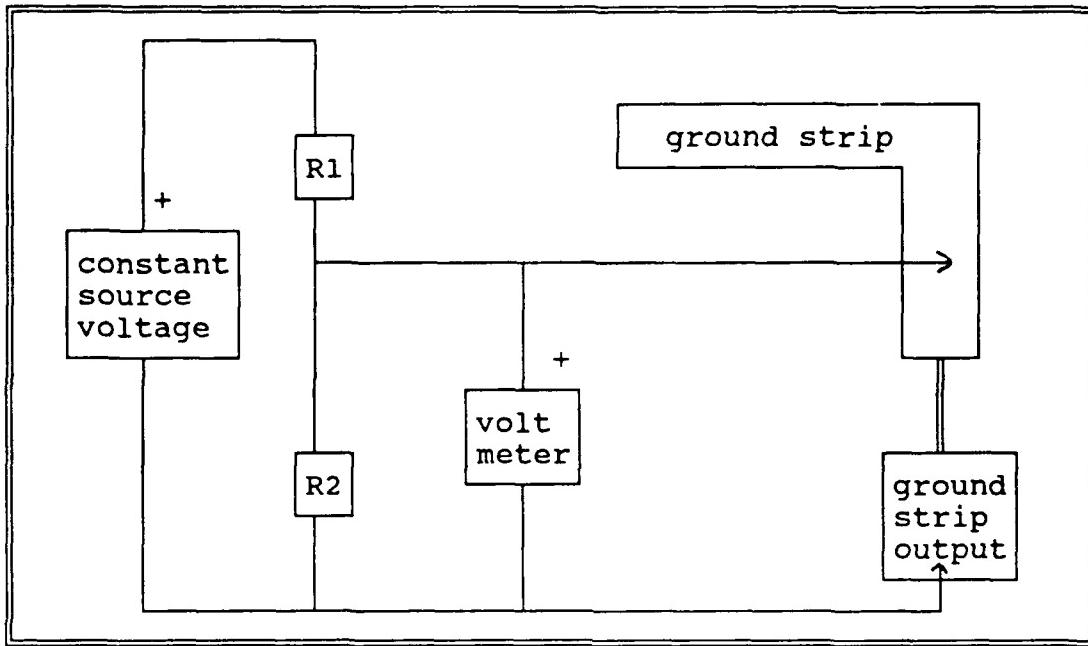


Fig. 6. Pad sensitivity test set-up to determine resistance of coated pad

Implantation

Time did not permit this section to be fully explored.

Wire Bonding. Testing was done to determine the correct operation of the wire bonder. These wires will be bonded to the chip power, control, and column output pads to the epoxy secured output leads.

For the wire bonder to work correctly the first bond was done using the lever and the second bond required the bond button to be pressed. The bond button bonded and cut the wire, then ejected a short piece of new wire for the next bond. The chip was placed at a height compatible with the bonding pin. Too high and the bond would not be secure; too low and the bonding pin pressure severed the wire.

Housing. Time did not allow testing of Takahashi's epoxy (Takahashi, 1987:157).

Previous Result Problems

These row select lines (#0, #1, #2) and double layer "PADs" were corrected on the MAGIC file: MONKEY5.MAG. The problem with Row #4 could not be located and was assumed to be a bonding problem because Szczublewski bonded each test chip by hand.

IV. RESULTS

Many processes were evaluated and modified. The brain chip electronics were tested, and they showed promising results. The metallization process allowed several chips to be overcoated with Au/Ni and Pt. Time did not permit complete examination of the ionic permeation and implantation procedures. The previous thesis problems were eliminated.

Brain Chip Electronics

The brain chip electronics were simulated correctly using the VLSI laboratory's simulation software. The actual MOSIS fabricated chips had many faults. The input, output, and line LABELS used in the text below refer to the labels used in the MAGIC file, MONKEY5.MAG.

False Power-up Test. This section is included to illustrate a common problem with proto-boards. The initial test showed a 25 mV drop across a resistor in-series with the supply voltage. This behavior indicated a 0.05 uA current flow. There were erratic outputs from the clock and other output leads. The problem was traced to a loose internal proto-board lead at the voltage input pin that created sporadic power flow.

Actual Test Results. With continuous power flow to the chips, the current, at 5 V, was typically around 10 Ma.

Clock. The 7-stage inverter clock, with divide-by-twos, was tested between 1.7 and 8 volts. It operated as a voltage controlled oscillator with the lowest clock speed at 39 KHz ($V_{dd} = 1.7$ V) and the highest above 1 Mhz ($V_{dd} = 8$ V). The clock speed over this voltage range appeared, on the oscilloscope, to change smoothly.

With a 5-volt source, the output at the 10th divider stage (divide by 1024) was approximately 110 kHz, indicating an oscillator frequency of 112.6 MHz.

Reset. The RESET enable (ENB) line was mistakenly not connected, but this had no effect on the RESET operation. ENB should have been grounded, this forces the I/O pad to operate strictly as an input.

The RESET line successfully connected the MUXED_OUTPUT line to the row 1, column 1 pad. This occurred on the negative transition of the CLOCK input. This behavior was confirmed first by observing that the two synchronizing signals, ROW_SYNC (row 1 selected) and COL_SYNC (column 1 selected), went high (V_{dd}). The second confirmation was obtained by applying a 5 V signal to various pads and noting the applied signal only appeared on the MUXED_OUTPUT line when the row 1, column 1 pad was used.

Multiplexers. Both row and column counters could not be operated simultaneously. Each operated correctly under specific conditions. Neither operated correctly at the target voltage: $V_{dd} = 5$ V.

At $V_{dd} = 5$ V, the binary row array selector lines, ra0 and ra1, had the same signal as the CLOCK input. Correct row operation of ra0 to ra3 was observed around certain source and CLOCK input voltages, and CLOCK frequencies (TABLE 1). To observe this operation, a minimum $1 \text{ M}\Omega$ input impedance was needed.

TABLE 1
PARAMETERS FOR CORRECT ROW ARRAY OPERATION

Source Voltage (V_{dd}):	CLOCK Input Voltage (V):	Clock Input Frequency (KHZ):
1.73	1.3	39
1.83	2.4	57.8
2	2	122.5
2.6	2.1	100
3	3.1	90
3.59	4.5	256

Cutting the row lines (ra0 to ra3) (see Fig. 7) to the multiplexer and setting V_{dd} at 5.6 V, the column counters were assumed to be operational. Correct operation was assumed by observing a 15 cycle delay between each COL_SYNC (column 1 selected) high output. Unfortunately at this voltage, the row counters could only manage a divide-by-two operation.

Capacitance between internal proto board connections and the external leads of the test pad influenced the row signals

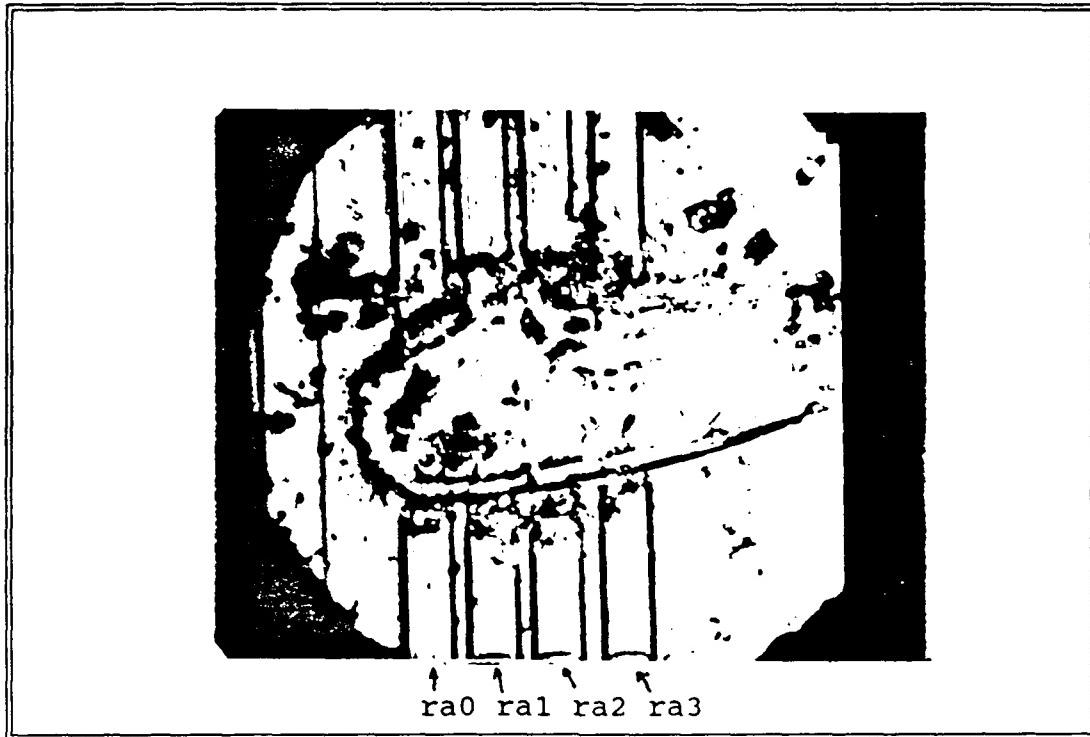


Fig. 7. Row address lines cut between counter and row select with acoustic cutter, contaminantes surround depression in substrate

(ra0 to ra3). These were reduced by locating the connections and leads away from each other.

Array Pad to Output Continuity. Continuity was confirmed, for the unprocessed (unmetallized) chip, on all row pads connected to the first column (column 1). Since all columns were identical in the MAGIC file, column 1 was chosen because it could easily be selected using the RESET line. The input signal was an 84 mV square wave at a frequency of 500 Hz. V_{dd} was varied between 3.6 V and 6.2 V, with the least noise (± 20 mV) on the output signal occurring at $V_{dd} = 5.4$ V. The output signal had the same shape as the input signal, but it was attenuated to a 60 ± 20 mV square pulse and shifted

down by 75 mV. This output signal was always detected at the column 1 output, no matter which of its rows were connected to the input signal. A similar output signal was also detected from the MUXED_OUTPUT, but only when the row 1, column 1 pad had the input signal. The cross-talk from a nonselected pad to either column 1's output or the MUXED_OUTPUT manifested a noise signal at -90 ± 20 MV, with no discernable pulse waveform. To decrease the noise a 5 k Ω load resistance should have been used

Latch-up. Latch-up was a continuing problem. The chip would sink sufficient current to melt the V_{dd} bond wire. These wires could withstand at least 0.7 A of continuous flow. Current limiting, power sources were used to minimize chip damage and to eliminate bond wire burn-out.

Static discharge caused some latch-up problems. The discharge sometimes occurred by touching the grounded micromanipulator table, changing probe locations, or moving test leads on the proto board.

Light also caused latch-up. Increasing the light intensity through the microscope lens, when it was focused near the multiplexers, sometimes caused latch-up.

Metallization

Masks. The mask making process was used to place the whole chip pattern into one mask. Some of the results discovered during this process are stated below.

Rubyolith Process. Knife cuts on the rubyolith did not appear on the 70 times reduced emulsion plate until the plates were extremely overexposed. A rubyolith mask was used to consolidate ground strip and array pads onto one mask, thus allowing mask alignment to be done with one alignment.

Reducers. Probably due to thermal contraction, the book setting for the rear box was not applicable. Instead, on two trials, the settings 67.7438 and 67.7579 were used with satisfactory results. Unfortunately, due possibly to reducer alignment and mask aligner problems, the created masks did not fit within the desired tolerance of a few microns. Nevertheless, the 10 μm overhang on the metallization mask allowed all of the Al pad to be covered.

Exposure times between 30 sec and 10 minutes were tried with the best time approximately 8 to 9 minutes. Shorter exposures did not sufficiently darken the plates, and longer exposures allowed reflections and rubyolith cuts to become noticeable.

Reverse Plate Copier. Copies of the Ernst and Sedlak mask were altered with rubyolith tape or water repellent ink and then successfully copied with the reverse plate copier. This procedure was accomplished so the pad array and ground strip could be separately mask aligned. This variation was necessitated because the ground strip and pad array were separated slightly more on the chip than on the mask.

Photomasks. Several photoresists were tried. Success was found using Shipley 1450J negative photoresist and either

an etchant or reverse lift-off procedure. The final specifications stated below in each section are the ones that facilitated a successful Au/Ni etch.

For Pt, a reverse lift-off procedure was used. This procedure required only application (without regard to meniscus) and softbaking.

Application. The initial spin speeds, used to apply the HMDS and the photoresist, were on the order of 3 and 4 krpm. To reduce meniscual build-up around the edges of the chips, a spin speed of 5 krpm was used. The shaft part os a cotton swab was carefully leaned against the edge of the chip and moved around it. This redirected the surface tension allowing the shaft to absorb some of the photoresist, thus reducing the meniscus.

Softbaking was done at 70 °C for 1 hour. Some sticking did occur.

Exposure. Exposure times from 2.5 to 10 minutes were tried. Seven minutes was found to be optimum. The highest points (meniscual edges) of the photoresist would press against the mask. This impeded mask alignment and full mask/surface contact.

Development. A developmen' spin speed of 500 rpm was found adequate. Slower speeds were tried such that the developing solution would build up a meniscual layer around the edges and develop more thoroughly there. The difference was not noticeable. Faster (over 1 krpm) speeds sometimes caused photoresist peeling.

The developer solution was Shipley 312A in a 4:3 solution in DIW. The development was stopped with a DIW rinse. Fig. 8 shows a well formed photomask over one of the electrode array pads. The wavy lines are interference patterns that reflect from a surface; the lines bend where there are depressions and elevations.

Two problems arose during the initial development procedure evaluation: (1) Complete removal of the photomask from the vias in the pads of Szczublewski's chips was not possible without damage to the other photomask areas. (2) The meniscual layer formed on the chip edges was quite large. The

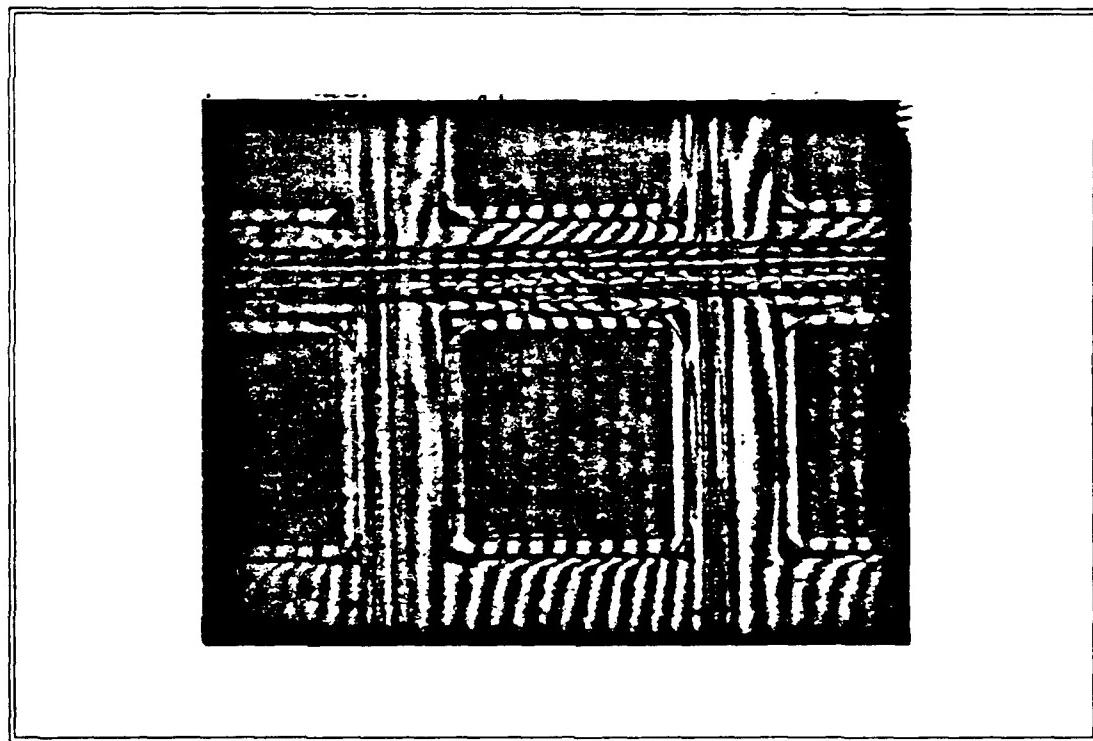


Fig. 8. Photomask formed around array pad, wavy lines indicate depressions and elevations, there is a square depression about $10 \mu\text{m}$ away from the metal (dark square) pad

unexposed areas near the center of the chip eroded before the exposed areas under the meniscual edge began to noticeably develop.

Sputtering. The actual sputtering time was approximately two to three hours. But the preliminary time (with no problems) was extrapolated to be around 5 to 6 hours, and is broken into: 2 hours for target set-up; 2 to 3 hours to cool down the cryogenic vacuum pump to operating temperature; and 1 hour to pump down to less than 5 microns of mercury.

The sputtering sessions were satisfactory. Fig. 9 shows a sputteren array pad. The lighter colored square indicated

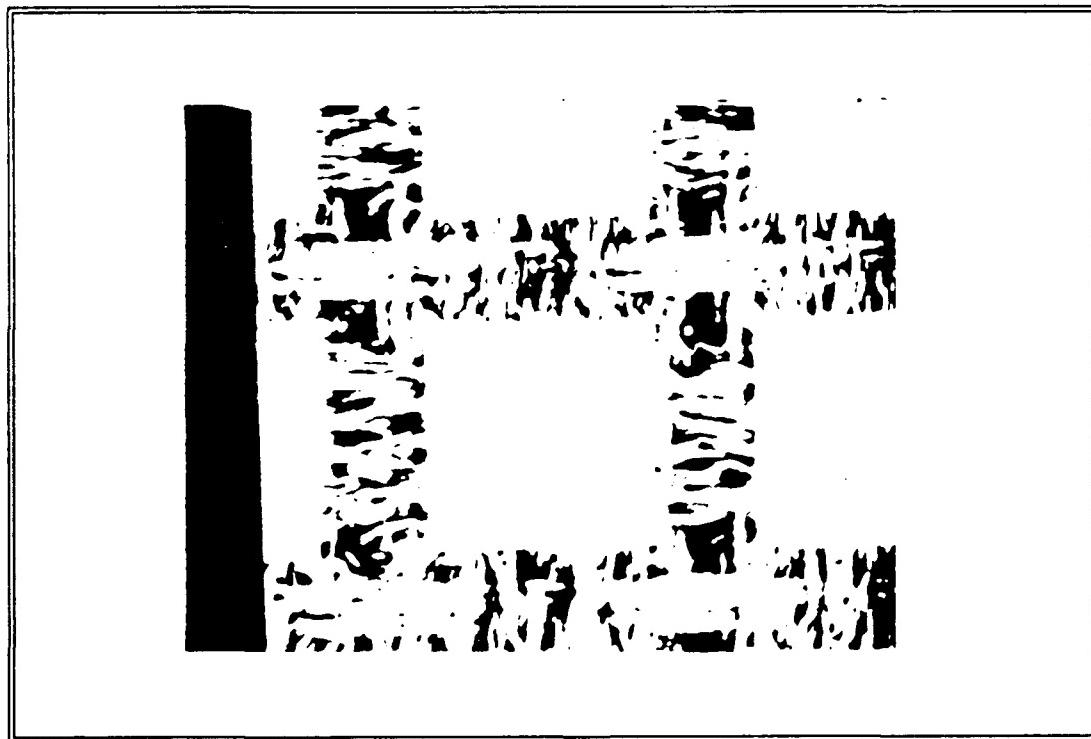


Fig. 9. Typical sputtering session, smooth coating on square array pad, wrinkled, poor adhesion to photomask area

a smooth layer of gold, whereas the wrinkled areas show that the gold and underlying photomask did not bond well, and should lift off easily. This was not the case (see Fig. 11)

Observations on target characteristics and contaminates are stated below.

Targets. Each metal had its own characteristic loading, tuning, forward and reflected powers, and Ar backpressure that allowed it to sputter (For typical values consult appendix: Sputtering). Au and Pt sputtered readily over a wide range of Ar backpressures. Ni was very difficult to sputter requiring higher Ar backpressure. If the Ar backpressure dropped, the copper plate holding the Ni would sometimes begin to sputter first. This seldom occurred with Au and Pt.

Contaminates. Sometimes the inside of the chamber would flake off landing on the chips or wafers. This was a much bigger problem than airborne gasses or particles becoming trapped within the sputtered metal. These particles created nonuniform landscapes that sometimes chipped off during subsequent processing. Examining several chips (at 8 x power) after Ni/Au sputtering and Surface Cleaning revealed contaminants, depressions and fissures on the pads (TABLE 2). Contaminants were also seen in similar numbers on non-pad areas.

TABLE 2
PAD SURFACES AFTER SPUTTERING AND CLEANING

Problems:	#/Chip
Fibers	1
Small Particles	1
Large Particles	2
Superficial depressions	7
Visible Depressions or Fissures	1

Pt coated pads had similar fiber and particle problems, but were depression free.

Other forms of contamination or incomplete sputtering were found. Blue-green spots appeared on the Au/Ni plated pads after a dilute solution of HCl was applied. (HCl was applied in an attempt to remove contaminants after an unsuccessful lift-off attempt.)

After a successful gold etch was performed, purplish areas were found on some pads (Fig 10).

Metal Removal. The lift-off procedure was not successful. Fig. 11 shows a partial lift-off of gold from between two array pads.

Two metal removal methods had partial success: a liquid etchant for Au; and a simple peel process for Pt.

Gold. The Au etch was also found to remove Ni and Al. The etching and photomask removal caused some pads to fragment and sliver. The Al was always left on the pads but sometimes bits of Au or Au/Ni were missing. Au/Ni slivers could also sometimes be seen around pad edges.

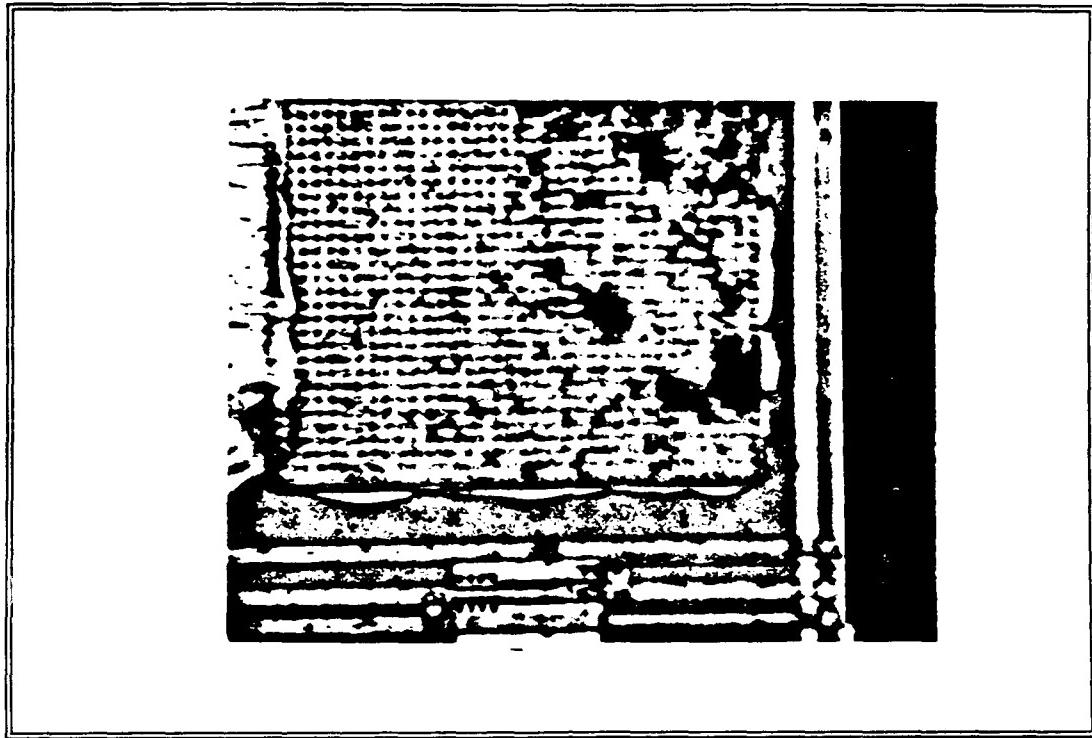


Fig. 10. Dark areas near center of picture are corrosion on the gold surface, the color is actually purple and AuAl_2 is suspected

Platinum. Tape lift-off of the Pt coating left 4 out of 5 chips with their Pt coated pads intact. On the fifth chip, the Pt coating was missing from a single pad (the Al was intact). This process did leave some slivers of Pt along the edges of the pads.

Also some pad lifting was evident on some chips. The first indication was an inability to focus on the full pad in the microscope. This was thought to indicate a bump (possibly contaminants in some cases). Pad lifting was confirmed on one pad during a height measurement. The DEKTAK II stylus profilometer was moved across this pad. The pad (under microscopic observation) moved down while the stylus was over



Fig. 11. Partial lift-off of gold between two pads, verticle silver lines are metal conductors within chip it and lifted up

after it passed. Also the height measurement showed a flat surface.

Metal Adhesion. Testing Au/Ni adhesion with Scotch tape on newly sputtered chips showed complete adhesion. Pt did not stick to the PSG. But, it did stick at least partially to 278 out of 279 Al pad areas on a chip. This was promising, and it was used as a lift-off procedure for Pt.

Pad Sensitivity. The electrometer revealed that the pad resistance of an unprocessed (no metal overcoating) chip to be approximately 5Ω . This reading was taken across the Al ground strip and ground strip output.

The impedance of the Pt pads was tested across the ground strip and ground strip output. The test configuration is shown in Fig. 6. Assuming the oscilloscope input impedance is much larger than the resistance across the pads, the pad resistance can be determined from the equation

$$R_{\text{pad}} = R_1 R_2 / ((R_1 + R_2) ((V_{\text{opened}}/V_{\text{closed}}) - 1))$$

where

R_1 = upper divider resistance

R_2 = lower divider resistance

$$R_1 + R_2 = 10 \text{ k}\Omega$$

V_{opened} = pads not connected

V_{closed} = pads connected.

The calculated pad resistance are shown below (TABLE 3).

TABLE 3

PAD RESISTANCE PARAMETERS (R_{pad} is calculated)

V_{opened} (mV):	V_{closed} (mV):	R_1 (Ω):	R_2 (Ω):	R_{pad} (Ω):
1.5 ± 6	1 ± 6	9980	20	40
3 ± 7.5	2 ± 7.5	9970	30	60
4 ± 1	3 ± 1	9970	30	88

Ionic Permeation

Polyimide. Takahashi's polyimide application process was not successful with chip implementation. The PI began to peel within seconds after development. Time did not permit further testing.

Implantation

Wire Bonder. Al wire bonding to Au/Ni pads was tested. Bonding was accomplished to even the smallest (100 μm by 100 μm , programmable I/O) pads. Time did not permit continuity checks.

Previous Result Problems

Previously observed problems were corrected. The three row select lines were added to the brain chip. All rows could be selected using the row address lines, or with specific V_{dd} and CLOCK values.

To eliminate the bumpiness of the interconnecting vias, MOSIS pads were created with a single metal--metal 2. Initial photolithography experimentation revealed that complete removal of the photoresist from the vias was not possible without damage to other photoresist coated areas.

V. CONCLUSION

By adding to Szcublewski's brain chip design and modified application of previous thesis chip processing, a finalized 16 by 16 brain chip was almost attainable within the thesis time constraints.

Brain Chip Electronics

Clock. The oscillator output was estimated to be 112.6 MHz. This is 61 % above the SPICE predicted output. A closer estimate (62.3 MHz) would occur if one divide-by-two circuit was operating incorrectly, as was seen in the resetable divide-by-two circuits. This does not seem to be the case because there were no observed jumps in clock speed as V_{dd} was transitioned from 1.7 V to 8 V. This indicated that the same number of divide-by-two circuits are always operational.

Reset. From the ENB circuit diagram (see fig), ENB only connects or disconnects the OUT line (from the chip electronics) buffer to the I/O pad. The diagram also shows a direct connection between the I/O pad and IN line (to chip electronics). Since the OUT line is not connected and, the chip I/O pad is connected directly to a power source, the unconnected ENB line should have little or no affect on RESET operation.

Counters. Possible reasons for the counter's erratic signals could be the following: (1) the addition of a RESET

transistor within each delay element; (2) capacitive, depletion effects from other chip elements and structures; (3) capacitive depletion effects from the metal and the substrate; (4) external capacitance through test leads. The most probable reason is (1).

Metallization

Masks. In general the mask process is useable. Some adjustments to the placement of the rear box on the variable reduces is needed to create a reduction closer to 70 to 1.

Photomasks. Softbaking probably did not sufficiently dry the photomask. This might not be the case, though, because problems with the meniscus sometimes caused excess pressure and scraping on the mask during alignment.

Contaminates. Dust was a continuing problem.

Greenish spots on the Au/Ni coated pads could be nickel-chloride formations. A fissure in the gold plating could have allowed the HCl to contact the nickel through capillary action.

The purplish spots discovered on the gold could have been a gold etch by-product, or possibly "purple plague."

Metal Adhesion. Metal adhesion to glass or quartz substrates seems to be related to the particular metal-oxygen bond strength (Cunningham, 1965:741). If metal-oxygen bonding is minimal, then the adhesion strength is primarily mechanical which is much less than metal-oxygen bonding.

The bond strength is related to the free energy formation of the metal oxide, listed as the "oxide formation" (with the units kcal) in the table: Metallic Constants. Ni, because of its negative formation energy, would seem to form strong oxygen bonds with PSG. Pt, on the other hand, because it does not bond well to SiO₂, probably only mechanically bonds to PSG. This would explain why it easily peeled from the non-metal (PSG) areas of the chip. The Au/Ni strips that slivered from the pad edges were probably undercut by the etchant.

Because the Au/Ni layer always adhered to Al (and PSG), a Ni interlayer of a few hundred angstroms is sufficient for adherence. Au/Ni fragmentation probably occurred through poor adhesion due to contaminants, etchant undercutting, or etchant seepage through holes in the photoresist.

The slivered or fragmented metal was pulled off mechanically by the photoresist's removal. This process included spinning the chip while spraying it with photoresist solvent, then rinsing it with DIW and drying it with N₂ gas.

Pad Sensitivity. The resulting ohmic impedance of the ground strip and pad output is very small and could be greatly influenced by noise. The small impedance measurements for Pt indicate a negligible interface barrier resistance.

Ionic Permeation

Array Pads. The usefulness of up-sizing and down-sizing the masks could be reduced because of inexact reductions of

the rubylith mask, undercutting during Au/Ni removal, and poor adhesion of the overhung Pt to the PSG.

Previous Result Problems

The previous thesis inability to select row 4 was attributed to a loose bonding wire, as these bonds were done by hand.

VI. RECOMMENDATIONS

Recommendations are not always meant to be taken at face value. Sometimes they represent the insight developed while nose to nose with an experiment gone awry. Sometimes they are just a best guess estimate. But they are suggestions that, given time, could have been explored.

Brain Chip Electronics

Amplifiers. To remove any possibility of a metal/metal barrier, and to increase the signal to noise (S/N) ratio, simple MOSFET amplifiers could be used. But this design will be linear over a very small range. Using operational amplifiers (opamps), a more linear signal increase could be attained. But the opamps might increase the chips heat output to an unacceptable level.

To fine tune each amplifier, on-chip or off-chip circuits can be built. The simplest design could include electrically erasable-programmable read-only-memory (EEPROM) current and voltage controllers.

Clock. Before the clock can be certified as working correctly, it should be checked, possibly with a voltage versus frequency graph. This would show if the divide-by-two elements are stable. Under certain conditions, some of the resetable divide-by-two elements simply passed a signal.

To allow frequency adjustments to the simple ring oscillator, a current controlling transistor between each inverter could be added (Haskard, 1987:146-148).

Delay Line Multiplexing. To separate and distribute brain chip electronics (for size and heat density reduction), the multiplexing of each column and row may be done with delay elements. Each individual column and row would contain a dedicated delay. A single "column-on" signal would circulate through the column delays. When the last column passes the "column-on" signal, it would also signal the row delays to pass the "row-on" signal to the next row delay.

Counters. A simple solution, that was operational in the clock circuit, was to eliminate the reset transistor. The reset transistor allows accurate synchronization during operational tests, but accuracy can still be maintained by recording both the clock and output signal simultaneously.

Metallization

Rubyolith Process. Because the masks do not need precise lines (\pm a few microns) and for easy modification, the rubyolith process should be replaced with computer graphics. A transparency may be created and photoreduced to the required size.

Metal Removal. Sometimes insufficient etchant passes into the small openings; in this case, gas reaction (plasma) etching has succeeded (Einspruch, 1986:190). Gas reaction

(plasma) etching could be explored to increase the yield of the Au/Ni coated chips.

Contaminants. Use of a dust filter is a necessity.

Annealing. The best annealing temperature and time could be found by observing the resistance changes during annealing tests. Information on metal/metal interactions between metal layers can be found in the following references:

Baglin, J. E. E. and J. M. Poate. Thin Film Phenomena: Interfaces and Interactions. Princeton, New Jersey: Electrochemical Society, 1978. page 129.

Poate, J. M., et. al. Thin Films-Interdiffusion and Reactions. New York: Wiley-Interscience, 1978. chapter 9.

The barrier height that remains (if any) may be estimated using I-V or C-V measurements (see Sharma, 1984).

Electropolishing. Chemically smoothing the pads might allow better contact to the cortex, and less possibility for corrosion or organic particle adhesion while in the CSF.

Platinum Black. Platinum may be converted to platinum black by immersion into a 3% platinum chloride solution containing 0.025% lead acetate (Mittal, 1982:1155). Platinum black is a highly corrosion resistant material and corresponds to a complete monolayer of hydrogen adsorbed onto the platinum's surface (West, 1970:55). The hydrogen helps to eliminate the formation of platinum oxide, a highly electrically resistive compound.

Appendix: Alloys

This appendix contains 5 equilibrium or phase diagrams of various of Al-Au, Al-Ni, Al-Pt, Au-Ni and Au-Pt alloys.

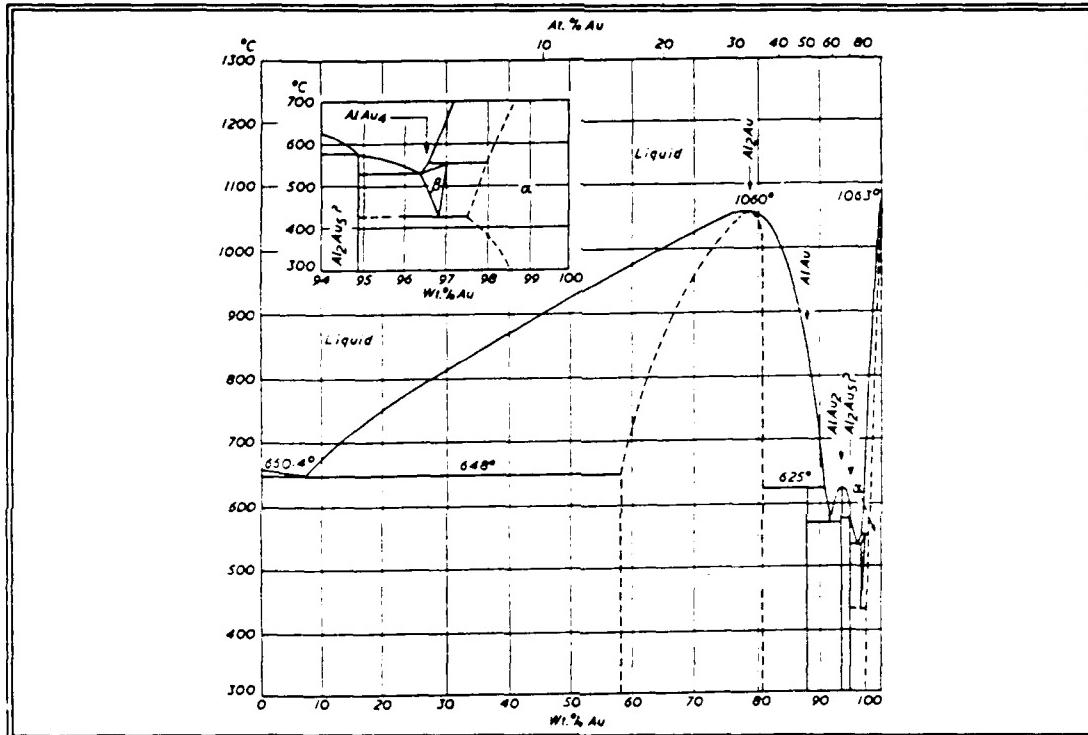


Fig. 12. Al-Au phase diagram (Smithells, 1976:393)

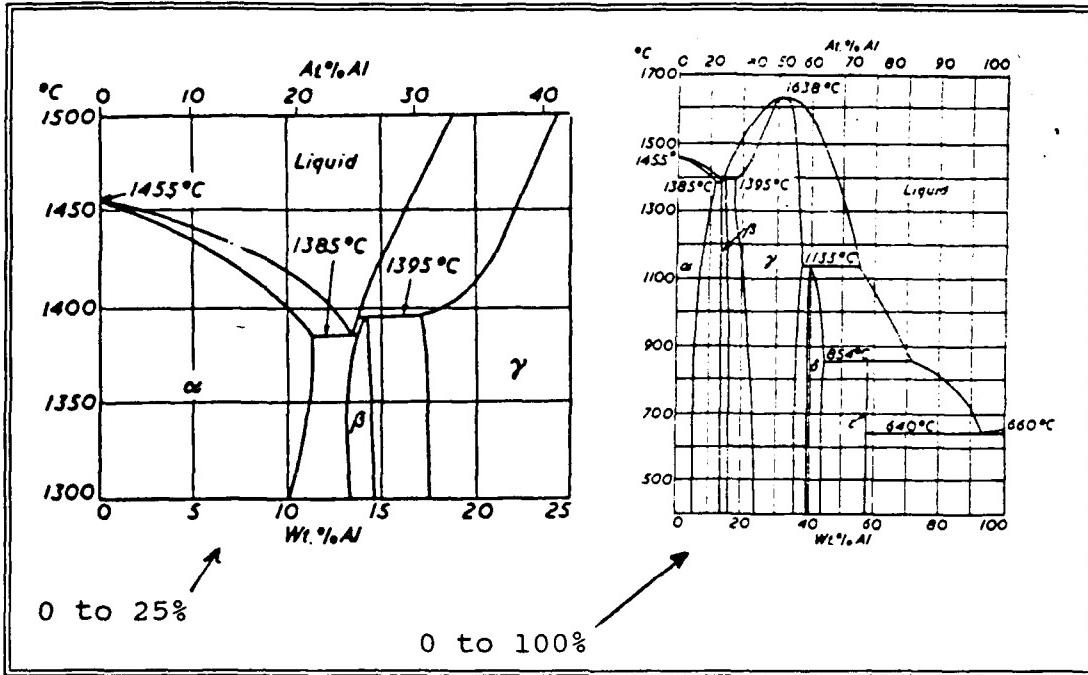


Fig. 13. Al-Ni phase diagram (Smithells, 1976:411)

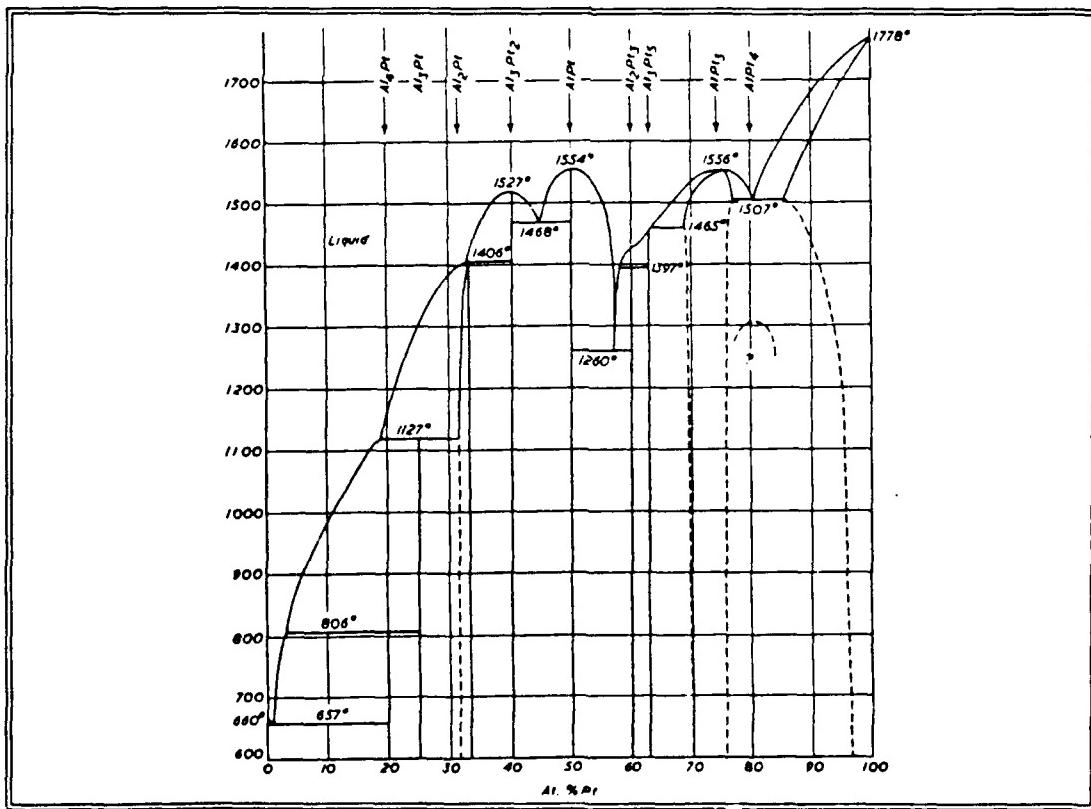


Fig. 14. Al-Pt phase diagram (Smithells, 1976:414)

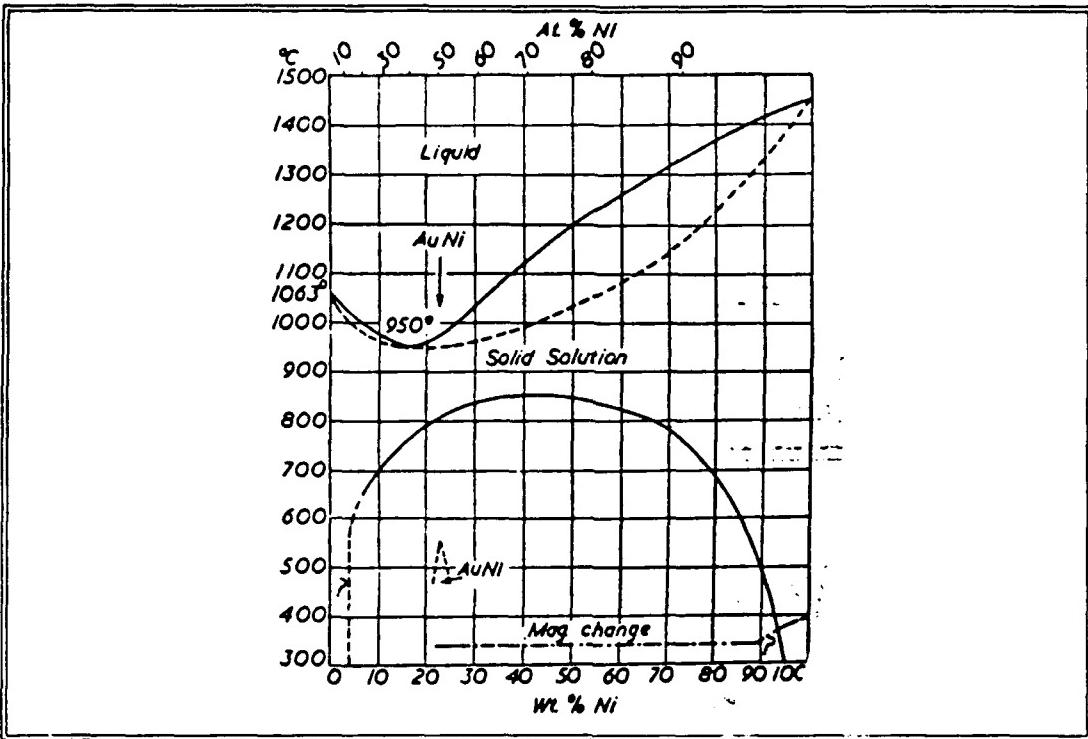


Fig. 15. Au-Ni phase diagram (Smithells, 1976:454)

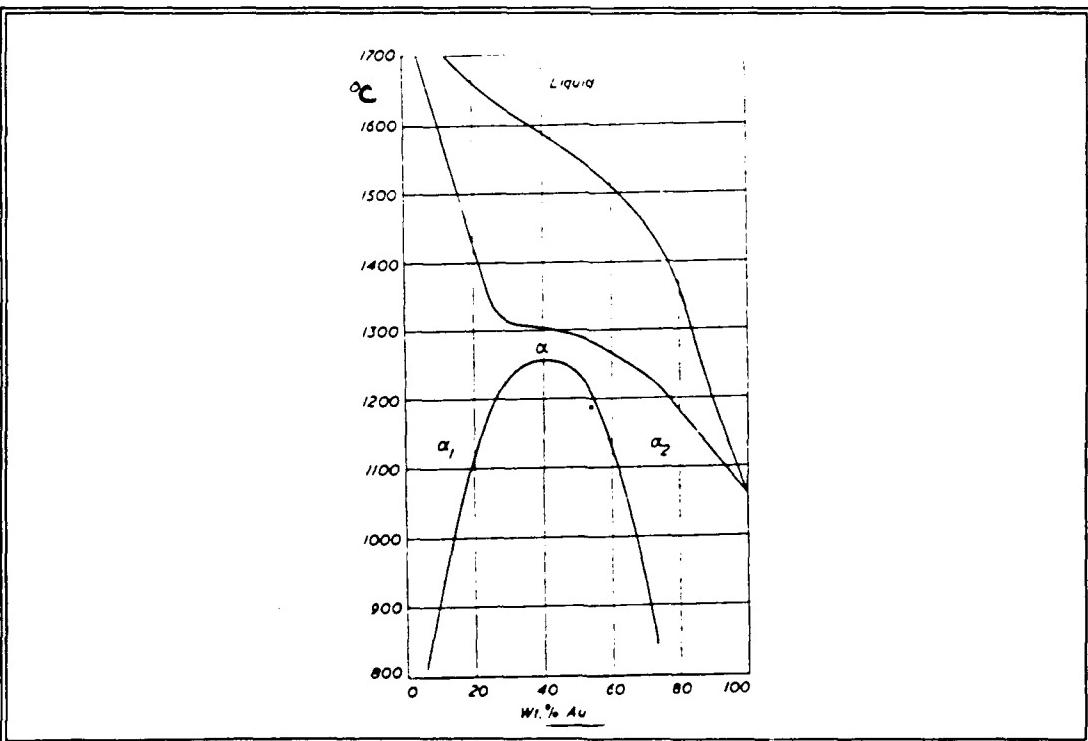


Fig. 16. Au-Pt phase diagram (Smithells, 1976:455)

Appendix: Equipment

The following sections contain information on the equipment used in this thesis. Within each section, the equipment is listed alphabetically.

Brain Chip Electronics

Acoustic Cutter. This device allowed micro-incisions on the order of a few of microns. This was done to remove unwanted connections on the MOSIS chip. The cut off (actually scratched off) metal and silicon substrate debris can cause unwanted connections to form. Clearing this debris by wiping, strong bursts of air, or rinsing with liquid can loosen bond wires. Softly blowing air or gentle immersion in DIW cleared the debris.

External Clocks. HP 3314A and Tektronic function generators.

Oscilloscopes. Both digital and analog oscilloscopes were used. The higher impedance inputs, allowed better operation of the chip counters.

Metallic Corrosion

DEKTAK II Profilometer. This device uses a diamond stylus to measure the height of a various surfaces.

Mask Aligner. The mask aligner is used to exposed the photomask to a UV light. It takes several minutes to fully warm-up once turned on. The nitrogen cooling flow to the lamp is critical and must be kept above 3.5 liters/min, to operate correctly.

Reducers. Two reducers were available, a fixed 10 to 1 step and repeat reducer and a variable (70 or less to 1) reducer. The step and repeat reducer requires a 2 inch by 2 inch image plate and will reduce and copy the image many times.

Reverse Plate Copier. This copier creates a reverse, mirror image of the original. Therefore, an exact copy requires two copies to be made, a copy of first copy. And a negative image, again, requires two copies with the second copy reverse developed.

Spinner. The spinner is used to allow uniform application of liquids over the whole wafer or chip. It also allows the liquids to partially dry after application. Before spinning, this device senses the vacuum pressure at the chuck opening. If the vacuum is not sufficient, for the selected spin speed, an alarm will sound and the spinner will refuse or cease to speed.

Thickness Monitor. To monitor deposition rates and estimate the thickness of sputtered materials while sputtering is in progress, the thickness monitor was used.

Implantation

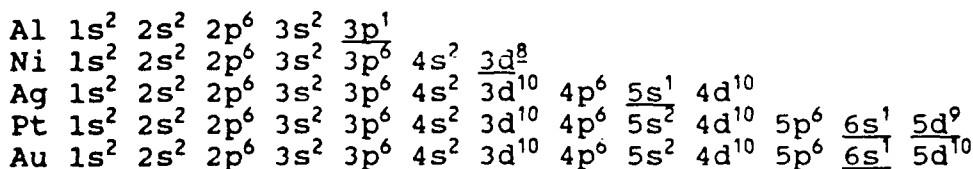
Wire Bonder. The wire bonder bonds the wires between the chip and the output leads. These are the 2 mil, diameter wires.

Appendix: Metallic Constants

All the metals listed below form face-centered-cubic structures containing 4 atoms per cell.

*	DESCRIPTION	UNITS	Ag	Al	Au	Ni	Pt
6	work function	eV	4.3	4.25	4.8	4.5	5.65
5	density	g/cc	10.5	2.7	19.3	8.9	21.5
2	melting point	°C	961	660	1063	1455	1774
5	lattice constant	Å	4.08	4.04	4.07	3.52	3.92
3	Si eutectic temperature	°C	830	577	370	964	830
1	free electron density	#/atom	1	3	1	.6	---
5	bulk resistivity	μΩ·cm	1.63	2.67	2.2	6.9	10.6
1	mean free path	Å	≈390	523	274	156	---
5	coefficient of expansion	---	19μ	24μ	14.4μ	13.7μ	9μ
2	oxide formation	kcal	-2.6	-376	39	-51.7	---
4	atomic weight	g/mole	107	27	197	59	195
2	adhesion to SiO ₂	---	low	high*	low	high	low
	acoustic impedance		---	---	23.18	26.68	36.0

(4*) The orbital electron configurations of the above elements are listed in order of ascending energy. The maximum number of electrons in each orbital type (s, p, d) are (2, 6, 10) respectively. Unfilled orbitals are underlined.



*Data reference sources:

- 1 = Chopra, 1969:69, 369
- 2 = Cunningham, 1965:742, 740
- 3 = Sharma, 1984:121
- 4 = Arya, 1976:257, 526
- 5 = Smithells, 1976:1029, 940
- 6 = Sze, 1981:396

Appendix: Sputtering

Below are the characteristics from various sputtering sessions. Each session is separated by a blank line. The deposition rate is calibrated to a tooling factor of 600%. 600% roughly corresponds to the half way point between the target, near the rim of the rotating table. The column headings and units are listed first.

- (1) Ar press (microns of mercury)
- (2) forward power (W)
- (3) reverse power (W)
- (4) deposition rate (Å/s)
- (5) load (-)
- (6) tune (-)
- (7) temperature (°C)

Metal:	(1)	(2)	(3)	(4)	(5)	(6)	(7)
Au	15	300	5	19.5	90	0	
	8.5	400	7	25.5	90	0	
	8.5	500	10	33	90	0	
	8.5	590	13	37.5	90	0	41
	10.5	404	7	25.5	90	0	
	6.5	404	7	27	90	0	
	5	404	7	28.5	90	0	
	3.5	404	7	28.5	90	0	
	2.6	404	7	30	90	0	
	1	404	7	30	90	0	
	.65	404	7	28.5	90	0	63
Au	2	410	7	26	90	35	
	1	410	7	28	90	35	
Au	6	250	4	21	92	32	
Au	12	250	4	10	92	25	
	6	250	4	12	92	25	
	5	500	10	26	88	33	
Au	30	500	23	13.3	76	3	
	16	500	23	24	76	3	
Ni	10	476	63	1	62	2	
	9	476	130	1	62	2	
Ni	15	401	86	1.3	77	4	
	12	500	110	1.3	77	5	
Pt	1	600	12	9.6	90	42	
	1	500	9	8.4	89	42	

Metal:	(1)	(2)	(3)	(4)	(5)	(6)	(7)
Pt	2	80	1	1.1	107	4	
	1.1	200	3	3.7	93	25	
	1.4	300	5	5.7	92	37	
	1.1	400	7	7.5	94	32	
	1	250	4	5	94	12	

Appendix: Standard Cleaning Schedules

WAFER CLEANING (Szczublewski, 1989:84): to remove surface chemical build-ups (such as oxides) and other contaminants.

Processed chips should not have this cleaning. Their oxides are used as insulators, and should not be removed. Also MOSIS chips have a phosphosilicate glass (PSG) barrier on their surface to eliminate unwanted surface oxides. Therefore, only a superficial surface cleaning is necessary (see below: SECONDARY CLEANING). Note the aluminum pads may have a detrimental oxide build-up and need the ALUMINUM CLEANING listed below.

soak in 1:1 ($H_2SO_4:H_2O_2$) for 15 minutes
- remove surface contaminants

rinse in DIW to $>10 M\Omega$
- ensures surface rinses clean

30 seconds in 4:1 (HF:ammonium fluoride)
- remove any surface oxidation

rinse in DIW to $>10 M\Omega$
- ensure surface rinses clean

dry in N_2
- removes surface moisture and "last" clinging material

bake overnight at 200 °C in N_2 atmosphere
- removes residual moisture and N_2 eliminates oxidation

ALUMINUM CLEANING: to remove aluminum oxide build-up on exposed pad areas. The HCl solution should not be used for a long period as it could seep under the MOSIS phosphosilicate glass and destroy the oxide insulation and metal lines.

dip into 1:10 (HCl:DIW)
- removes oxide and roughens Al surface for better metal adhesion

rinse in DIW
- surfactant to dissolve and reduce surface tension of oxide particles

dry with N_2
- mechanical action to remove particles

spin dry at 4 krpm for 30 seconds
- to remove residual water

AT THIS POINT FOLLOW: SURFACE CLEANING (below)

SURFACE CLEANING: to remove surface contaminants only. Note ALUMINUM CLEANING (above) could be used first if needed.

while spinning at least 1 krpm do the following:
- mechanical action to remove particles

rinse with acetone
- surfactant to dissolve and reduce surface tension of particles

dry with N₂
- mechanical action to remove particles

rinse with methanol
- surfactant to dissolve and reduce surface tension of particles

dry with N₂
- mechanical action to remove particles

rinse in DIW
- surfactant to dissolve and reduce surface tension of particles

dry with N₂
- mechanical action to remove particles

spin dry at 4krpm for 30 seconds
- removes residual water

bake 1 hr at 200 °C in N₂ atmosphere
- removes residual moisture and N₂ eliminates oxidation

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Vita

Captain Pierre K. LeFevre was born in the Queen of Angels Hospital, Los Angeles, California on March 31, 1957. The son of Theodore R. and Hideko T. LeFevre graduated from Arroyo High School, in El Monte, in 1975. He attended the California Polytechnic State University at San Luis Obispo, whereupon, in 1983, he received a Bachelor of Science in Physics. After graduation, he entered the USAF and attended OTS in San Antonio, Texas. His first assignment was to attend the University of New Mexico at Albuquerque, through the Undergraduate Conversion Engineering Program. This was his first Air Force Institute of Technology (AFIT) program. Graduating with a Bachelor of Science in Electrical Engineering in 1986, he was assigned to the 1000th Satellite Operations Group at Offutt AFB, Omaha, Nebraska. During his three years there, he preevaluated launch and early orbit test procedures, analyzed satellites' states of health, devised critical energy conservation method for orbiting systems, and devised many quick-fix solutions for realtime satellite emergencies. Selected again to attend AFIT, he entered the School of Engineering, in May 1989.

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13. ABSTRACT (Maximum 200 words) This research furthered the processing steps of the AFIT 16 by 16 implantable cortical semiconductor integrated circuit electrode array, or brain chip. The areas of interest include the brain chip electronics, metallization, ionic permeation, and implantation. The electronics and metallization are heavily covered. A high speed, single clock divide-by-two circuit was modified with a reset transistor and cascaded to form a ripple counter. This device had stable operation at specific source voltage and clock voltage and frequency. A cascaded 7-stage inverter with 10 unmodified divide-by-two circuits operated between 1.7 and 8 volts, and between 39kHz and 1MHz, respectively. The metallization process refers to coating Au/Ni or Pt onto exposed aluminum areas(pads) of a CMOS integrated circuit. Sputtering was used to coat the chip. And an Au/Ni etchant or Pt peel-off technique was used. The Au/Ni etchant was iodine, potassium iodide, and deionized water. Pt removal was accomplished by simply peeling the Pt back from the chip. Pt adheres to Al, but not to phosphosilicate glass (PSG). The basic phenomena and operation of rubylith mask generation, photomasking, and annealing are discussed in detail.			
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